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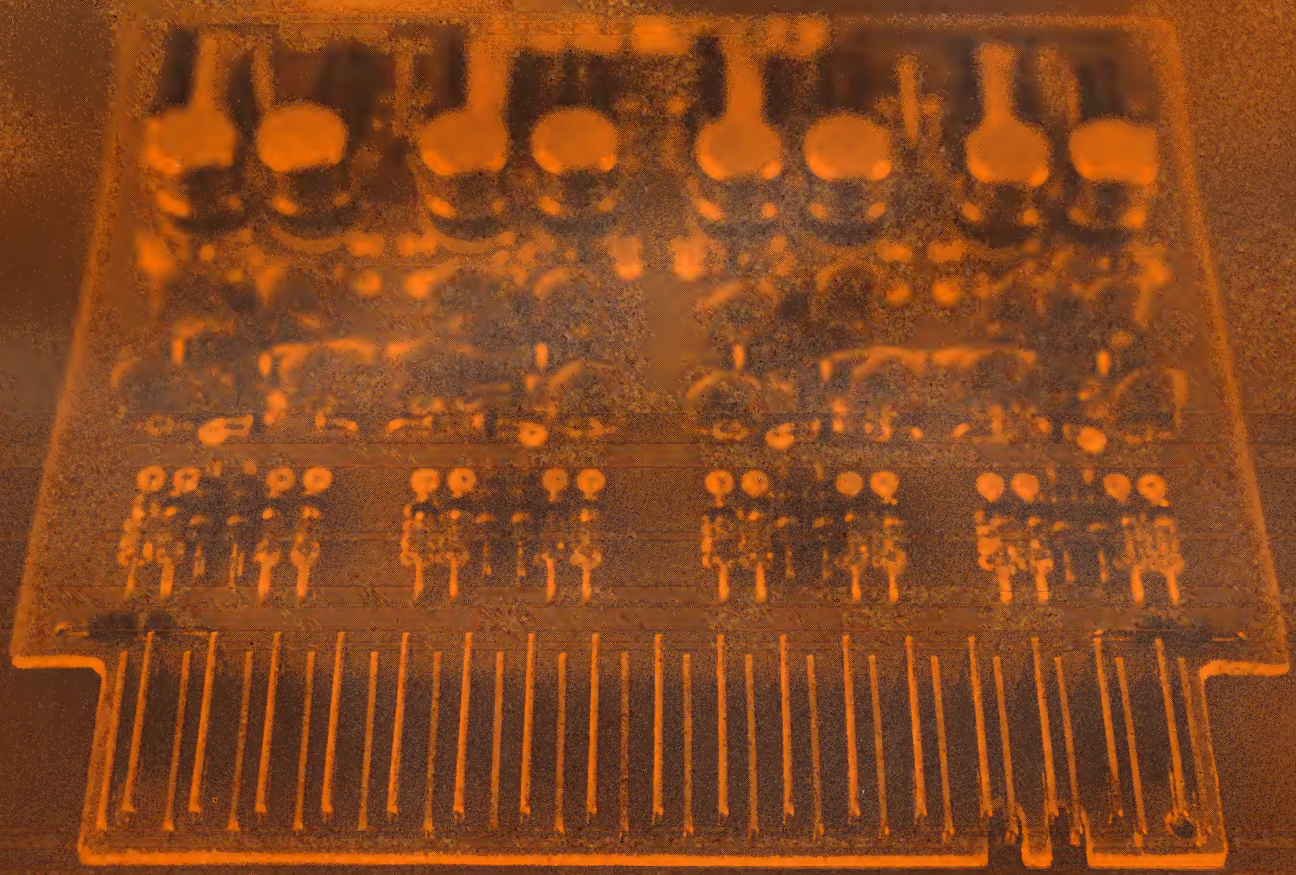
RAYTHEON COMPUTER

G-SERIES DIGITAL CIRCUIT MODULES



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RAYTHEON

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NEW IN THIS CATALOG

This new edition of Raytheon Computer's G-Series Module Catalog contains a number of important additions, including a series of 20 MC modules and the complete contents of the 1965 Catalog Supplement (SP-191). New modules in this catalog include a versatile half adder, reed relays and silicon switches and a series of analog modules: two digital-to-analog converters, a reference voltage supply and a voltage comparator.

In addition, the center supplement contains data on a Diode AND/OR Gate; a Gated Driver; a Shift Register, and a Digital Multiplexer.

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G-SERIES 35 PIN DIGITAL CIRCUIT MODULES

INTRODUCTION Raytheon Computer has designed and offers a completely compatible line of "off the shelf" low-cost, high quality germanium digital modules for 200 KC, 1 MC, 5 MC and 20 MC frequencies. This line of logic modules has been especially engineered in these frequencies for applications in computer logic, digital systems, logical control systems, telemetered data reduction, and data processing and information handling systems. In addition, a series of special modules —all directly compatible with the four frequencies— are available.

RELIABILITY All Raytheon Computer modules are manufactured under MIL-Q-9858 requirements and are 100% tested prior to customer delivery. Based on operating systems, Raytheon Computer digital circuits have a mean-time-to-failure in excess of 1 million hours. Transistors are used at no more than 75% of rated voltage and current. Diodes have a 2 to 1 voltage safety margin. Government Source Inspection can be supplied on request, for a nominal handling charge. Raytheon Computer is under the cognizance of the U.S. Navy Government Inspector.

COMPATIBILITY Modules in the 200 KC, 1 MC, and 5 MC frequencies are similar in circuit design and logic function. All cards are identical in mechanical structure and electrical circuitry. Engineering features such as epoxy (fiberglas) material, test points, wave soldering, and noise rejection are included in each design series. All modules have the same logic levels; 0 volts equals binary 0; –9 volts to –12 volts equals binary 1. All germanium modules are "keyed" for ease of installation and removal. Operating temperature range is between 0°C and 55°C. The 20 MC modules have different electrical circuitry, but are compatible with all standard Raytheon modules.

NORMAL LOGIC Incorporated in Raytheon Computer's digital modules are "normal logic" circuits as opposed to "clamped logic" techniques. The use of normal logic increases circuit reliability by preventing damage during accidental shorting or removal of module while power is on. Normal logic circuits require fewer components; thus increasing the reliability factor and reducing the cost for each card. *Typical noise rejection for Raytheon Computer circuits is 3 volts.*

MODULE ECONOMICS Occasionally digital design engineers ask why Raytheon Computer doesn't offer more variations of the same type of circuit. For example, why isn't a diode AND gate module offered with two input gates or why aren't more varieties of flip-flops provided?

The answer to this question is Raytheon Computer's desire to offer a customer the best circuit design at the lowest possible price.

Each circuit is designed to be more useful for a variety of applications. Incorporated is a multi-functional design which gives a customer more capability per card. A customer therefore may purchase fewer different circuits per application.

Not only does a customer purchase fewer circuits but each card he does buy is lower priced than others in the industry. This is due to total reduced engineering design time and less production tooling, inventory, and personnel.

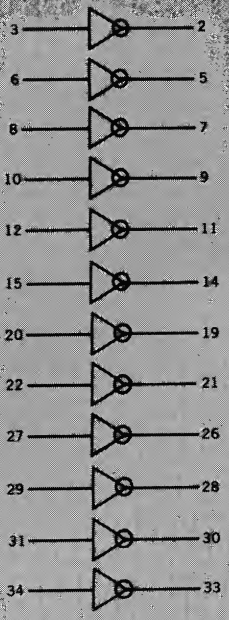
In the end it is the customer who benefits with lower prices, 30% to 60% per circuit.

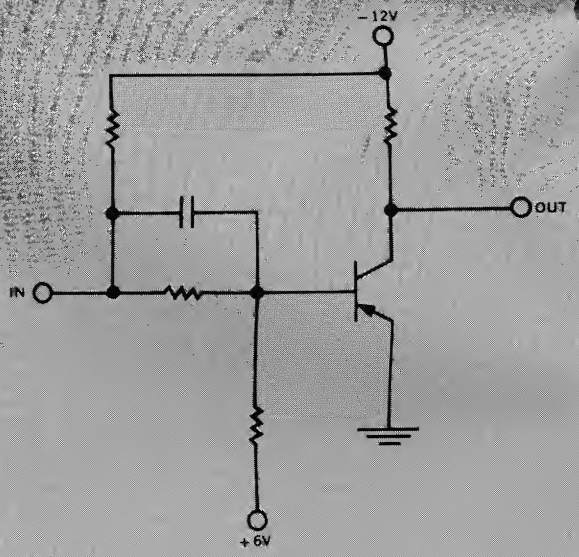
FIVE YEAR WARRANTY Raytheon Computer warrants all standard modules to be free from any defects. If within five years from delivery any module fails in normal service due to defective material or poor workmanship and the purchaser notifies the company immediately, Raytheon Computer will replace the module without charge. This warranty is on the module and not the customer; therefore if a customer builds equipment using Raytheon Computer modules and passes the equipment on to a third party, the warranty continues to the third party. In addition, if a module is damaged due to misuse or misapplication, Raytheon Computer will repair or replace the unit for a nominal charge, not to exceed 50% of the original price.

DELIVERY For prompt module delivery Raytheon Computer maintains over $500,000 of digital circuit cards in its inventory. Typical delivery from stock for flip-flops, diode gates, counters, inverters, etc., can be made within 24 to 48 hours.

GAI2
AMPLIFIER-INVERTER

KEY SLOTS PINS 19, 21





The GAI2 Amplifier Inverter has 12 independent logic inverter circuits. When the input is binary one, the output is binary zero. When the input is binary zero, the output is binary one. In addition, the GAI2 provides logic level restoration and improves degraded rise times.

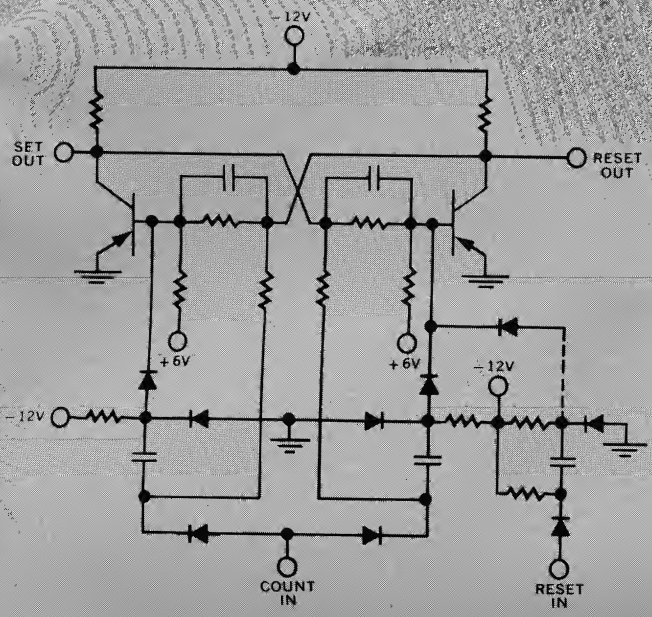
The GAI2 is also useful as a heavy duty, non-inverting gate driver or flip-flop driver. Connect the output of one inverter to the input of one or more other inverters. Use the second inverter as a non-inverting driver.

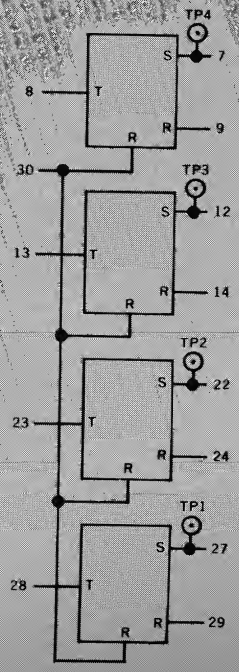
NOTE: When operating the GAI2 at less than ½ maximum rated frequency the drive capability for capacitive loads is doubled.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
AMPLIFIER INVERTER	**GAI2-.2**	**GAI2-1**	**USE GDI1-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	
Voltage Levels			
One (—10V nominal)	—8 to —12V	—8 to —12V	
Zero (0V nominal)	+1 to —1V	+1 to —1V	
Max. Rise Time	2.5μs	0.4μs	
Max. Fall Time	2.5μs	0.4μs	
Input Load	1 N load 5 P loads 1 C2 load	1 N load 5 P loads 1/2 C1 load	
Noise Rejection Min. Noise input for output disturbance less than 2.0V	1.5V	1.5V	
OUTPUT			
Voltage Levels (full load) One Zero	—9 to —12V +.5 to —.3V	—8 to —12V +.5 to —.3V	
Max. Rise Time (No load)	0.3μs	0.1μs	
Max. Fall Time (No load)	0.5μs	0.2μs	
Max. Rise Time (Full load)	1.0μs	0.25μs	
Drive Capability (See Note 1)	30 N loads 12 P loads 4 C2 loads	9 N loads 16 P loads 2 C1 loads	
With 390Ω load resistor on output of GA12-.2 (returned to —12V)	6 N loads 45 P loads 10 C2 loads		
With 1K load resistor on output of GAI2-1 (returned to —12V)		4 N loads 30 P loads 5 C1 loads	
Max. Wiring Capacity	1000 pf	500 pf	
PROPAGATION DELAY	0.15μs	60ns	
POWER REQUIREMENTS			
per card —12V (pin 32) +6V (pin 4) Gnd (pin 18)	187ma 3.6ma	187ma 3.6ma	

NOTE 1: When driven by the GDG2-1 AND gate the GAI2-.2 drive capability is 20 N, 12 P, 4 C2.





GBC1
BINARY COUNTER
FOUR STAGE

KEY SLOTS PINS 17, 29

THE GBC1 has four toggle flip-flops which can be interconnected in such a way as to count in straight binary fashion from 0 through 15. Connect the set output of each flip-flop to the toggle input of the next flip-flop. The output of the last flip-flop provides an N/16 output — one pulse out for each 16 into the GBC1 input. True and false outputs are available for all four flip-flops providing 8-4-2-1 and $\overline{8}$-$\overline{4}$-$\overline{2}$-$\overline{1}$ outputs. Each circuit is triggered by the trailing edge (positive going) of a negative pulse. Any number of modules may be connected in series to form a multi-stage counter.

A preset value may be entered into the counter by external switches connected to the output of each flip-flop. When the switch is momentarily connected to ground (OV), that flip-flop output goes to binary 0 (OV). For high speed presetting, a solid state switch such as a relay driver, lamp driver or inverter may be used.

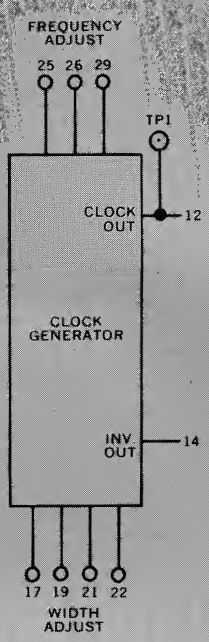
The positive going portion of a negative pulse into the reset input resets all four (4) flip-flops.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
BINARY COUNTER	**GBC1-.2**	**GBC1-1**	**GBC1-5**
INPUT			
Voltage Levels			
One (—10V nominal)	—9 to —12V	—8 to —12V	—7 to —12V
Zero (0V nominal)	+1 to —1V	+1 to —1V	+1 to —1V
Count Input			
Trigger (positive step)			
Minimum amplitude	8V	8V	7V
Maximum rise time	1μs	0.25μs	60ns
Minimum dwell at binary one level	2μs	0.4μs	80ns
Maximum repetition rate	200 Kc	1 Mc	5 Mc
Input Load	1 N load	1 N load	2 N loads
Reset Input			
Trigger (positive step)			
Minimum amplitude	8V	8V	7V
Maximum rise time	1μs	0.25μs	60ns
Minimum dwell at binary one level	10μs	2μs	0.5μs
Reset Input Load	1 N load ½ C2 load	1 N load ½ C1 load	2 N loads ½ C5 load
Noise Rejection	2V	2V	1.5V
Min. positive noise input for output disturbance of less than 0.5V			
OUTPUT			
Voltage Levels (full load)			
One (—10V nominal)	—9 to —12V	—8.0V to —12.0V	—7.0V to —12.0V
Zero (0V nominal)	0 to —0.25V	0 to —0.3V	0 to —0.3V
Maximum rise time (no load)	0.25μs	0.1μs	30ns
Maximum fall time (no load)	0.5μs	0.2μs	50ns
Maximum rise time (full load)	1μs	0.25μs	50ns
Drive Capability	8 N loads 5 P loads 2 C2 loads	8 N loads 6 P loads 2 C1 loads	12 N loads 7 P loads 2 C5 loads
Maximum wiring capacitance per output	1000pf	300pf	50pf
PROPAGATION DELAY	.4μs	0.2μs	100ns
From 10% of rising count input to 10% of rising output of most significant bit (full load on outputs of msb).			
POWER REQUIREMENTS			
per card			
—12V (pin 32)	60ma	80ma	100ma
+6V (pin 4)	1.8ma	1.5ma	2ma
Gnd (pin 18)			

GCG1
CLOCK GENERATOR

KEY SLOTS PINS 15, 19

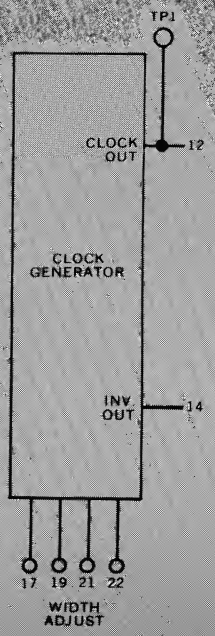


The GCG1 Clock Generator is a free-running oscillator intended for use as a system master clock. In addition to the normal clock output, the inverted output is available.

The frequency set at the factory is approximately one half the maximum rated frequency. To increase the frequency to maximum, jumper pins 25 and 26. To decrease the frequency (with or without pins 25 and 26 jumpered) connect a capacitor from pin 29 to gnd (pin 18). The duty cycle may be adjusted by jumpering pins 17 and 21 for operation at near one-half the maximum rated frequency and by jumpering pins 17 and 22 for operation near one-fifth the maximum rated frequency.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
CLOCK GENERATOR, (tuneable)	**GCG1-.2**	**GCG1-1**	**GCG1-5**
OUTPUT			
Frequency	20 Kc to 200 Kc	200 Kc to 1 Mc	1 Mc to 5 Mc
Voltage Levels			
One (Nominal −10V)	−10 to −12V	−10 to −12V	−7 to −12V
Zero (Nominal 0V)	+.2 to −.3V	+.2 to −.3V	+.5 to −.7V
Maximum rise time (no load)	0.25μs	0.1μs	15ns
Maximum fall time (no load)	0.5μs	0.2μs	50ns
Maximum rise time (full load)	1.0μs	0.25μs	50ns
Duty factor adjustment	45% to 55%	45% to 55%	45% to 55%
Drive capability			
Clock Out	15 N loads 100 P loads 15 C2 loads	12 N loads 100 P loads 12 C1 loads	20 N loads 180 P loads 10 C5 loads
Inv. Out	3 N loads 0 P loads 0 C2 loads	2 N loads 0 P loads 0 C1 loads	2 N loads 0 P loads 0 C5 loads
Temperature Stability	±2%	±2%	±2%
Maximum wiring capacitance	1000pf	500pf	100pf
POWER REQUIREMENTS			
per card			
−12V (pin 32)	45ma	45ma	45ma
+6V (pin 4)	3ma	3ma	3ma
Gnd (pin 18)			



GCG2
CLOCK GENERATOR

KEY SLOTS PINS, 15, 19

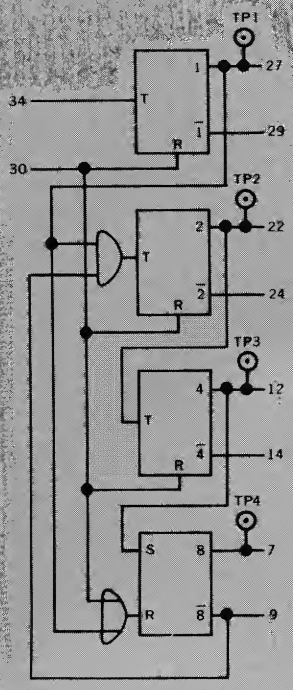
The GCG2 Clock Generator is a crystal-controlled oscillator intended for use as a system master clock where frequency stability is required. The output circuitry is identical to the GCG1. The circuit will operate at any crystal frequency within the specified limits. When ordering the GCG2, the operating frequency should be specified. Adjustment of the duty cycle is identical to the GCG1.

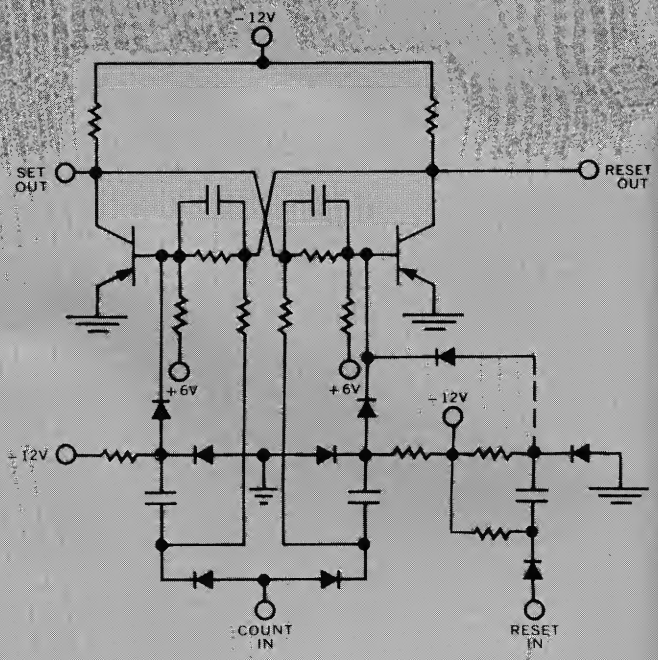
SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
CLOCK GENERATOR (crystal controlled)	**GCG2-.2**	**GCG2-1**	**GCG2-5**
OUTPUT			
Frequency	40 Kc to 200 Kc	200 Kc to 1 Mc	1 Mc to 5 Mc
Voltage Levels			
One (nominal −10V)	−10 to −12V	−10 to −12V	−7 to −12V
Zero (nominal 0V)	+.2 to −.3V	+.2 to −.3V	+.5 to −7.V
Maximum rise time (no load)	0.25μs	0.1μs	15ns
Maximum fall time (no load)	0.5μs	0.2μs	50ns
Maximum rise time (full load)	1μs	0.25μs	50ns
Duty factor adjustment	45% to 55%	45% to 55%	45% to 55%
Drive capability			
Clock Out	15 N loads 100 P loads 15 C2 loads	12 N loads 100 P loads 12 C1 loads	20 N loads 180 P loads 10 C5 loads
Inv. Out	3 N loads 0 P loads 0 C2 loads	2 N loads 0 P loads 0 C1 loads	2 N loads 0 P loads 0 C5 loads
Temperature Stability	±.005%	±.005%	±.005%
Overall frequency stability	±.02%	±.02%	±.02%
POWER REQUIREMENTS			
per card			
−12V (pin 32)	45ma	45ma	45ma
+6V (pin 4)	3ma	3ma	3ma
Gnd (pin 18)			

GDC1
DECADE COUNTER

KEY SLOTS PINS 15, 31





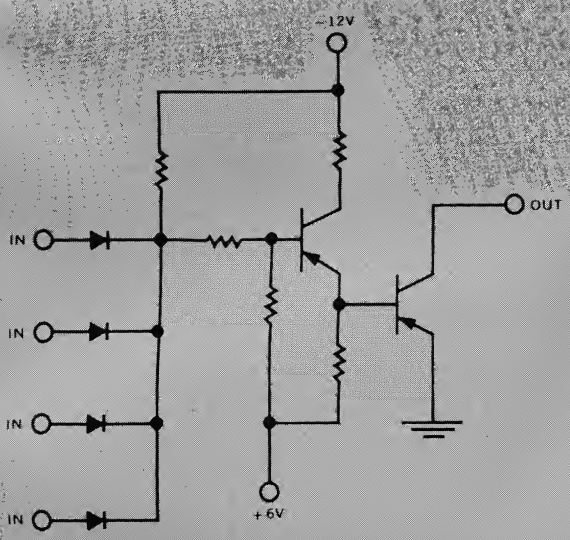
The GDC1 decade counter has four (4) flip-flops interconnected with internal gating in such a way as to count from 0 through 9. The output of the last flip-flop provides an N/10 output — one pulse out for each 10 into the GDC1 input. True and false outputs are available for all four (4) flip-flops providing 8-4-2-1 and $\overline{8}$-$\overline{4}$-$\overline{2}$-$\overline{1}$ outputs. The true output of each flip-flop is internally wired to serve as the carry signal to the succeeding stage. Each circuit is triggered by the trailing edge (positive going) of a negative pulse. Any number of modules may be connected in series to form a multi-stage counter.

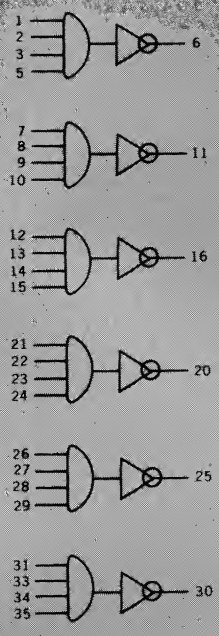
A preset value may be entered into the counter by external switches connected to the output of each flip-flop. When the switch is momentarily connected to ground (OV), the flip-flop output goes to binary 0 (OV). For high speed presetting, a solid state switch such as a relay driver, lamp driver or inverter may be used.

The positive going portion of a negative pulse into the reset input resets all four (4) flip-flops. A.C. reset must be delayed at least 2 μsec from the input clock pulse.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
DECADE COUNTER	**GDC1-.2**	**GDC1-1**	**GDC1-5**
INPUT			
Voltage Levels			
One (—10V nominal)	—9 to —12V	—8 to —12V	—7 to —12V
Zero (0V nominal)	+1 to —1V	+1 to —1V	+1 to —1V
Count Input			
Trigger (positive step)			
Minimum amplitude	8V	8V	7V
Maximum rise time	1μs	0.25μs	60ns
Minimum dwell at binary one level	2μs	0.4μs	80ns
Maximum repetition rate	200 Kc	1 Mc	5 Mc
Count Input Load	1 N load	1 N load	2 N loads
Reset Input			
Trigger (positive step)			
Minimum amplitude	8V	8V	7V
Maximum rise time	1μs	0.25μs	60ns
Minimum dwell at binary one level	10μs	2μs	0.5μs
Reset Input Load	1 N load ½ C2 load	1 N load ½ C1 load	2 N loads ½ C5 load
Noise Rejection Min. positive noise input for output disturbance of less than 0.5V	2V	2V	1.5V
OUTPUT			
Voltage Levels (full load)			
One (—10V nominal)	—9 to —12V	—8 to —12V	—7 to —12V
Zero (0V nominal)	0 to —0.25V	0 to —0.3V	0 to —0.3V
Maximum rise time (no load)	0.25μs	0.1μs	30ns
Maximum fall time (no load)	0.5μs	0.2μs	50ns
Maximum rise time (full load)	1μs	0.25μs	50ns
Drive Capability	7 N loads 5 P loads 2 C2 loads	6 N loads 8 P loads 2 C1 loads	10 N loads 7 P loads 2 C5 loads
Maximum wiring capacitance per output	1000pf	300pf	50pf
PROPAGATION DELAY From 10% of rising count input to 10% of rising output of most significant bit (full load)	0.4μs	0.2μs	100ns
POWER REQUIREMENTS			
per card			
—12V (pin 32)	60ma	80ma	100ma
+6V (pin 4)	1.8ma	1.5ma	2ma
Gnd (pin 18)			





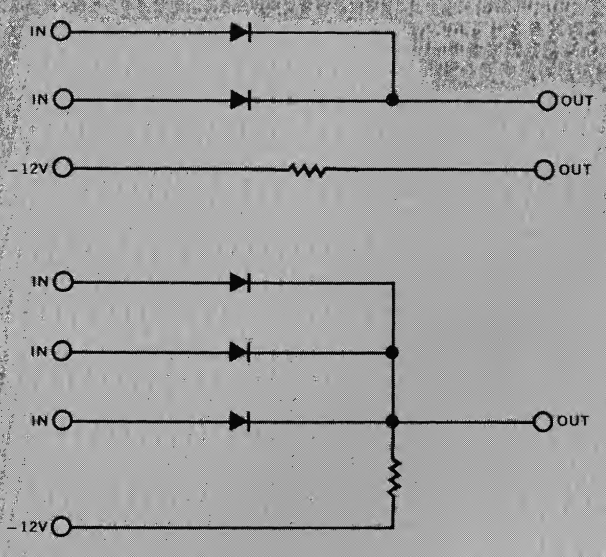
GDD1
DISPLAY DRIVER

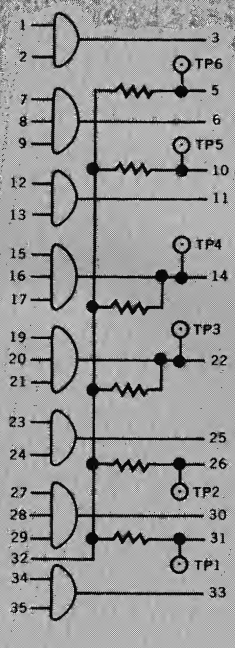
KEY SLOTS PINS 9, 29

This module consists of six identical and independent drive circuits. Each circuit has a four-term diode AND gate and two amplifier stages. The four-term diode gate can be used as decoding matrix for binary or Gray coded four digit inputs. Thus, any binary or Gray coded input can be used, and a desired decoding is obtained by proper interwiring on the connector socket. Two GDD1 modules may be used to give twelve outputs for driving filament lamps in the projection "in-line" display.

SPECIFICATIONS

MODULE	
DISPLAY DRIVER	**GDD1**
INPUT	
Frequency	0 to 2 Kc
Voltage	
One (−10V nominal)	−7 to −12V
Zero (0V nominal)	+1 to −1V
Current	
One	2.2ma
Zero	−0.14ma
Input Load	1 N load
OUTPUT	
Voltage	−28V max.
Current	
Resistive Loads	500ma max.
Incandescent Lamps (Steady State)	250ma max.
POWER REQUIREMENTS per card	
−12Vdc (pin 32)	395ma
+ 6Vdc (pin 4)	9ma
Gnd (pin 18)	





GDG2
DIODE AND GATE

KEY SLOTS PINS 5, 17

The GDG2 has four (4) two-input and four (4) three-input DC AND gates. For maximum versatility, six (6) of the gates are not connected to a load resistor. To make AND gates with more than three inputs, connect the outputs of two or more gates together. An AND gate with up to 12 inputs may be made in this manner. Regardless of the number of inputs, the output of the AND gate should be connected through a single load resistor to —12V.

Example: To make a 5-input AND gate, connect pins 3, 5 and 6 together.

When an AND gate is used to drive another AND gate or any other N type load, the load resistor of the first (driving) gate may be left unconnected. A maximum of two GDG2 AND gates may be connected in cascade (series).

AND/OR logic using the GDG2 AND gate and GDG3 OR gate may be cascaded indefinitely.

One of the inputs to the GDG2 AND gate may be used as an OR output. This OR output may be connected to the node of the GDG3 OR gate.

NOTE: The 1MC AND gate is also used with the 200 KC units. Slight differences in specifications are indicated for compatibility with the 200 KC line.

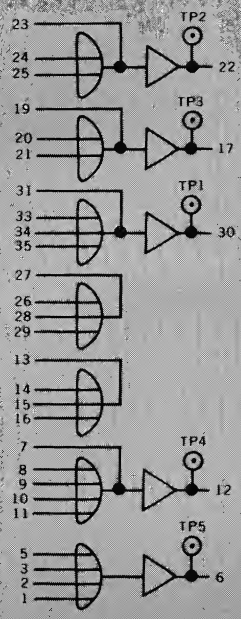
SPECIFICATIONS

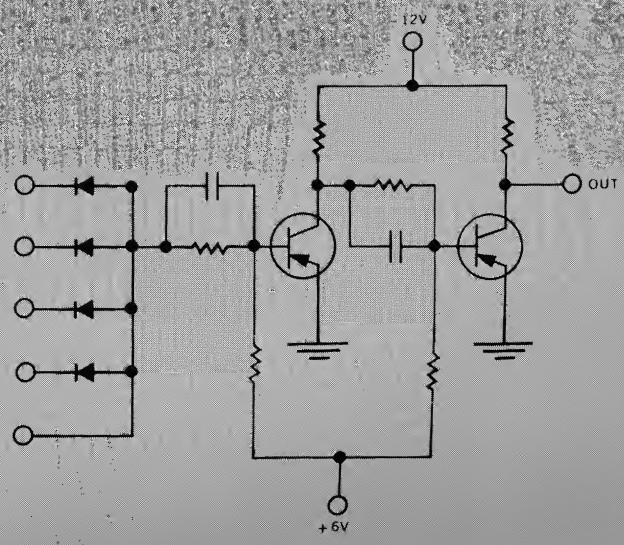
MODULE	200 KC	1 MC	5 MC
DC AND GATE	**GDG2-1**	**GDG2-1**	**GDG2-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (—10V nominal)	—9 to —12V	—8 to —12V	—7 to —12V
Zero (0V nominal)	+1 to —1V	+1 to —1V	+1 to —1V
Maximum rise time	1μsec	0.25μsec	60ns
Input Load (nominal)	1 N load*	1 N load*	2 N loads*
OUTPUT			
Voltage Levels (full load)			
One (—10V nominal)	—9 to —12V	—8 to —12V	—7 to —12V
Zero (0V nominal)	+.5 to —1V	+.5 to —1V	+.5 to —1V
Rise time (full load)	Same as input	Same as input	Same as input
Fall time (no load)	Same as input	Same as input	Same as input
Typical Level Shift (output from input)	—0.5V	—0.5V	—0.5V
Drive Capability	10 N*	10 N*	10 N*
	2 P	3 P	8 P
	1 C2	1 C1	1 C5
Driving Inverters	The AND gate is suitable for driving one Inverter such as the GAI2, GDI1 or GDI2. Because the output voltage level of an AND gate driving an Inverter is shifted out of tolerance for other circuits no loads should be driven in addition to the inverter.		
Maximum wiring capacitance	1000pf	300pf	50pf
PROPAGATION DELAY	10ns	10ns	10ns
POWER REQUIREMENTS			
per card			
—12V (pin 32)	13ma	13ma	30ma
+6V (pin 4)	0	0	0
Gnd (pin 18)			

*All N type loads driven by the GDG2 AND gate must be added to the input load of the driver AND gate. For example, if an AND gate is driving 5 other AND gates, each with an input load of 1 N type load, then the effective input load of the first gate is 6 N (1 + 5).

GDG3
DC OR GATE

KEY SLOTS PINS 15, 33





The GDG3 DC OR gate is comprised of two 2-input, one 3-input, and two 4-input DC OR gates and two 3-input diode clusters. The output of either or both of the clusters may be connected to the node of the other gates to provide DC OR gates of five to ten inputs.

The dual inverter amplifier output of the GDG3 OR gate restores logic levels and waveforms. Each amplifier is designed to reject variations in the logic levels of the input signals. This eliminates the normal disadvantage of diode gating and increases the reliability of standard easy-to-use AND/OR logic. When using the GDG3 OR gate, DC AND/OR gates may be cascaded indefinitely.

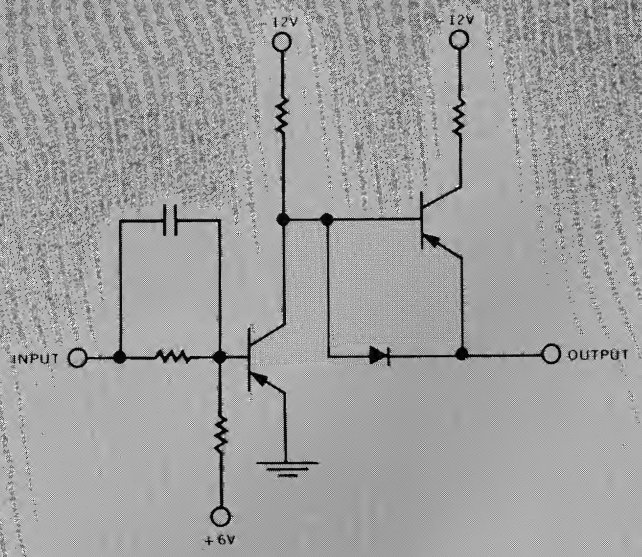
Any circuits not used as OR gates may be used as non-inverting amplifiers.

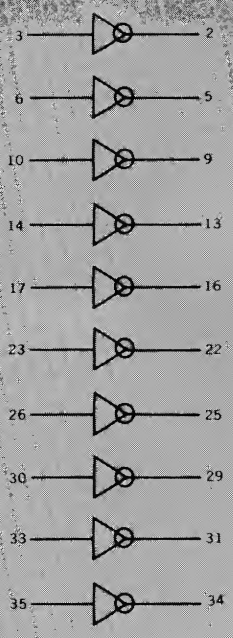
Outputs of the GDG3 OR gate may be ANDed merely by connecting them together. A maximum of three outputs may be connected in this fashion to provide an OR/AND output giving, for example, the maxterm expression (A+B) (C+D) (E+F+G+H). When outputs are connected together in this fashion, the drive capability for N loads is reduced to three (3).

NOTE: When operating the GDG3 at less than ½ maximum rated frequency the drive capability for capacitive loads is doubled.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
OR GATE	**GDG3-.2**	**GDG3-1**	**GDG3-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (nominal −10V)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (nominal 0V)	+1 to −1V	+1 to −1V	+1 to −1V
Maximum Rise Time	2.5μs	0.4μs	100ns
Input Load	2 P loads	3 P loads	4 P loads
Noise rejection	1.5V	1.5V	1.5V
OUTPUT			
Voltage Levels (full load)			
One (nominal −10V)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (nominal 0V)	0 to −0.3V	0 to −0.5V	0 to −0.5V
Maximum Rise Time (no load)	0.3μs	0.1μs	40ns
Maximum Fall Time (no load)	0.5μs	0.2μs	100ns
Maximum Rise Time (full load)	1μs	0.25μs	60ns
Drive Capability	15 N loads 10 P loads 3 C2 loads	10 N loads 12 P loads 3 C1 loads	15 N loads 15 P loads 3 C5 loads
Maximum Wiring Capacitance	1000pf	300pf	50pf
PROPAGATION DELAY	0.2μs	0.1μs	50ns
POWER REQUIREMENTS per card			
−12Vdc (pin 32)	69ma	69ma	110ma
+ 6Vdc (pin 4)	2.2ma	2.2ma	5ma
Gnd (pin 18)			





GDI1
DRIVER INVERTER

KEY SLOTS PINS 17, 19

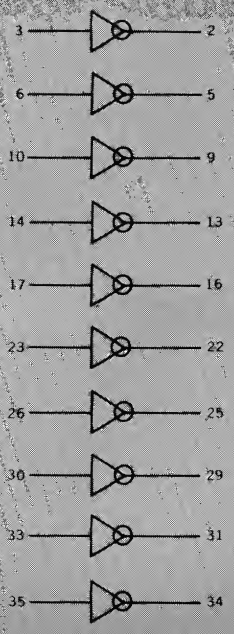
The GDI1 has 10 independent driver inverter circuits. These circuits are useful as universal drivers. Each circuit has an inverter driving a PNP emitter follower with a by-pass diode around the emitter follower. Connected in this fashion, the circuit has all the driving advantages of both the inverter and the emitter follower without the disadvantage of either. This is an excellent all around driver for capacitive loads, resistive loads returned to a negative voltage and resistive loads returned to a positive voltage. It has a low output impedance for both positive going and negative going signals and offers very good isolation between the load and the circuit driving into the inverter.

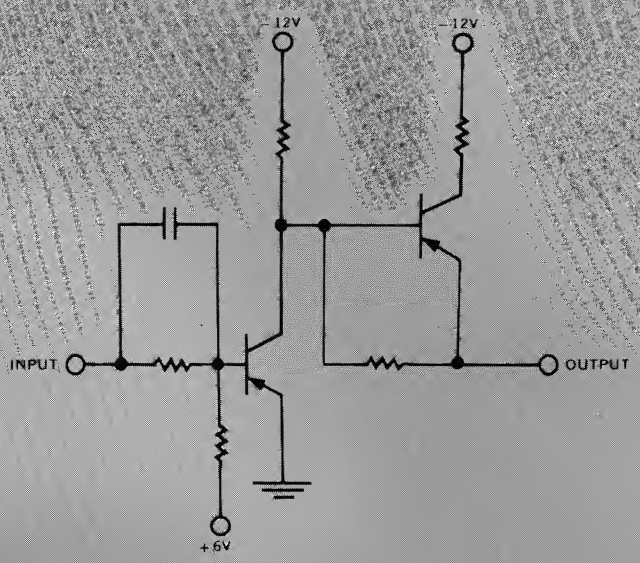
SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
DRIVER INVERTER	**GDI1-.2**	**GDI1-1**	**GDI1-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (−10V nominal)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (0V nominal)	+1 to −1V	+1 to −1V	+1 to −1V
Maximum rise time	2.5μs	0.4μs	100ns
Maximum fall time	2.5μs	0.4μs	100ns
Input Load (nominal)	7 P loads 1 C2 loads	7 P loads ½ C1 load	9 P loads ½ C5 load
Noise Rejection	1.5V	1.5V	1.5V
OUTPUT			
Voltage Levels (full load)			
One (−10V nominal)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (0V nominal)	+.5 to −.7V	+.5 to −.7V	+.5 to −.7V
Maximum rise time (no load)	0.25μs	0.1μs	30ns
Maximum fall time (no load)	0.5μs	0.2μs	50ns
Maximum rise time (full load)	1.0μs	0.25μs	30ns
Drive Capability			
Driven by AND Gate (where the GDI1 is the only load on the AND gate)	6 N loads 100 P loads 6 C2 loads	7 N loads 100 P loads 7 C1 loads	20 N loads 180 P loads 10 C5 loads
Driven by Flip-Flop Type Circuit (FF, OS, SR, ST)	17 N loads 100 P loads 17 C2 loads	12 N loads 100 P loads 12 C1 loads	20 N loads 180 P loads 10 C5 loads
Driven by GDI1 or GCG1 or GCG2	30 N loads 100 P loads 40 C2 loads	20 N loads 100 P loads 20 C1 loads	20 N loads 180 P loads 10 C5 loads
Maximum wiring capacitance	1000pf	500pf	100pf
PROPAGATION DELAY in chain of inverters between consecutive outputs	0.25μs (load: 1000pf to gnd)	0.1μs (load: 500pf to gnd)	15ns (load: 100pf to gnd)
POWER REQUIREMENTS			
per card			
−12V (pin 32)	100ma	100ma	90ma
+6V (pin 4)	5ma	4ma	4ma
Gnd (pin 18)			

GDI2
DRIVER INVERTER
CABLE DRIVER

KEY SLOTS PINS 17, 19





The GDI2 has 10 independent driver inverter circuits capable of transmitting digital data over distances of 1500 ft. at the maximum specified frequency. Termination resistors are internally connected.

The GDI2 will drive shielded or unshielded twisted pair, or coaxial cable. If several twisted pairs are being driven, it is recommended that they be separated or separately shielded to eliminate cross-coupling effects. If coaxial cable is used, 93 ohm is recommended for the best impedance match.

For short runs (under 50 ft.), the logic circuit at the cable termination may be driven directly by the GDI2. When driving logic directly the external termination resistor should not be connected. For longer runs, it is recommended that the GDR1 Data Receiver be used at the cable termination.

NOTE: When driving long cables with the GDI2 Driver Inverter, the circuit output may appear to be garbled. This is due to the reflected waveform of the transmitted signal and does not affect operation of the driver. The speed of signal transmission in the cable is approx. 1.5 nsec per foot of cable. The signal reflection travels a complete round trip and appears on the output of the Driver Inverter approximately 3 nsec per foot after the signal is transmitted.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
DRIVER INVERTER	**GDI2-.2**	**GDI2-1**	**GDI2-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (—10V nominal)	—9 to —12V	—8 to —12V	—7 to —12V
Zero (0V nominal)	+1 to —1V	+1 to —1V	+1 to —1V
Max. Rise Time	2.5μs	0.40μs	100ns
Max. Fall Time	2.5μs	0.40μs	100ns
Input Load	7 P loads 1 C2 load	12 P loads ½ C1 load	12 P loads ¼ C5 load
Noise Rejection	1.5V	1.5V	1.5V
OUTPUT			
Voltage Levels	See Note 1	See Note 1	See Note 1
One (Nominal —10V)	—9 to —12V	—8 to —12V	—7 to —12V
Zero (Nominal 0V)	0 to —0.3V	0 to —0.5V	0 to —0.5V
Max. Rise Time (Full load)	0.2μs	80ns	60ns
Max. Fall Time (Full load)	0.8μs	120ns	75ns
Drive Capability through 50 ft. of Twisted Pair or 93Ω coaxial cable.	8 N loads 80 P loads 6 C2 loads	4 N loads 80 P loads 6 C1 loads	10 N loads 80 P loads 5 C5 loads
With over 50 ft. of cable the GDI2 can drive 1 GDR1 data receiver.			
PROPAGATION DELAY	.25μs	.1μs	15ns
POWER REQUIREMENT			
per card			
—12V (pin 32)	184ma	180ma	259ma
+6V (pin 4)	2.5ma	5.5ma	4.4ma
Gnd (pin 18)			

GDL1
DELAY LINE

KEY SLOTS PINS 3, 23

The GDL1 consists of a delay line with built-in write and read storage elements at its input and output respectively.

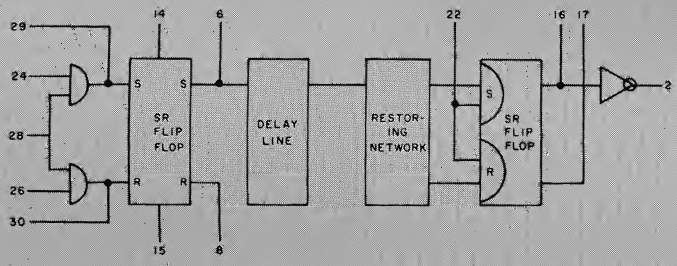
An input signal when fed into the write storage element is propagated through a magnetostrictive delay line. (A delay of up to 1300 μsec is available as required by customer.) This delayed signal is then amplified and carried through into the read storage element where the signal is synchronized (Pin 22) with an external clock frequency to insure that the delayed signal is in sync with the original input frequency.

An inverter amplifier is connected at the output to provide buffering between output and load.

Delay adjustment is ±1 μs. The length and width of the GDL1 is the same as standard cards. This module requires 3 card spaces.

NOTE: If pins 24 and 26 are not used for input gating they should be connected to pins 8 and 6 respectively to provide J-K steering.

NOTE: Pins 8 and 6 should not be loaded. They are to be used only with pins 24 and 26 to provide J-K steering.



SPECIFICATIONS

DELAY LINE INPUT:	GDL1-1
Frequency	0 to 1 Mc
Voltage Levels	
One (—10V nominal)	—8 to —12V
Zero (0V nominal)	—1.0 to 1.0V
Rise Time	0.25μsec
Clock Input Load	4 N Loads
Set, Reset Input Load	1 N Loads
Noise Rejection	1.5V
OUTPUT: (Pins 8 & 17)	
Voltage Levels (full load)	
One (—10V nominal)	—8 to —12V
Zero (0V nominal)	0 to —.3V
Rise Time (no load)	0.1μsec
Fall Time (no load)	0.2μsec
Rise Time (full load)	0.25μsec
Drive Capability	9 N Loads 9 P Loads 2 C1 Loads
OUTPUT: (Pin 2)	
Voltage Levels (full load)	
One (—10V nominal)	—8 to —12V
Zero (0V nominal)	0 to —0.3V
Rise Time (no load)	.1μsec
Fall Time (no load)	.2μsec
Rise Time (full load)	.25μsec
Drive Capability	10 N loads 5 P loads 2 C1 loads
OUTPUT: (Pin 16)	
Voltage Levels (full load)	
One (—10V nominal)	—8 to —12V
Zero (0V nominal)	0 to —0.3V
Rise Time (no load)	0.1μsec
Fall Time (no load)	0.2μsec
Rise Time (full load)	.25μsec
Drive Capability	9 N loads 2 C1 loads
Power Requirements (per card)	
—12V (pin 32)	124ma
+6V (pin 4)	13ma
Gnd (pin 18)	

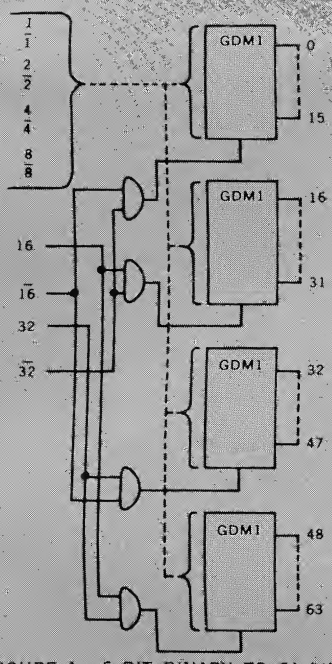
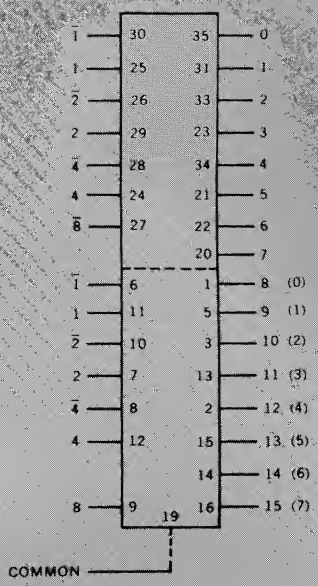


FIGURE 1 — 6 BIT BINARY TO 64 LINE CONVERSION



GDM1
DECODING MATRIX

KEY SLOTS PINS 15, 17

The GDMI Decoding Matrix contains sixteen (16) four-input AND Gates prewired to provide 4-bit binary to 16 line decimal code conversion.

An auxiliary gate expansion input is included and prewired and effectively causes all gates to operate as five input gates. This allows connection of two or more GDM1 with a small amount of additional logic to provide 32, 38, 64, 128, — outputs. This auxiliary input can also be used as an inhibit to turn off the entire board.

For example a six-bit binary code may be converted to 64 line decimal as shown in Fig. 1.

In addition, the GDM1 is wired so that each card may be used as two separate binary or binary coded octal to octal converters. In a large decoding matrix even though the 1, $\overline{1}$, 2, $\overline{2}$, 4, $\overline{4}$, 8 and $\overline{8}$ are connected to more than one GDM1, the loading effect is the same as one GDM1 because only one matrix is enabled at a time. Thus a decoding matrix with 10 GDM1 may be driven from a single flip-flop or inverter.

NOTE: If the auxiliary input is not used, it must be connected to —12V. Connect unused outputs to gnd. to reduce input drive requirements.

NOTE: The 1MC Decoder Matrix is also used with the 200 KC units. Slight differences in specifications are indicated for compatibility with the 200 KC line.

NOTE: The GDG3 OR gate is an excellent circuit to use as an output for the GDM1.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
DECODING MATRIX	**GDM1-1**	**GDM1-1**	**GDM1-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (Nominal —10V)	—9 to —12V	—8 to —12V	—7 to —12V
Zero (Nominal 0V)	+1 to —1V	+1 to —1V	+1 to —1V
Maximum rise time	1μs	0.25μs	60ns
Input Load (per pin)	4 N loads*	4 N loads*	8 N loads**
Common Input Load	4 P loads	4 P loads	8 P loads
OUTPUT			
Voltage Levels (full load)			
One (Nominal —10V)	—9 to —12V	—8 to —12V	—7 to —12V
Zero (Nominal 0V)	See Note 1	See Note 1	See Note 1
Maximum rise time (full load)	Same as input	Same as input	Same as input
Maximum fall time (no load)	Same as input	Same as input	Same as input
Drive Capability	0 N loads	0 N loads	0 N loads
See Note 2	2 P loads	3 P loads	5 P loads
	1 C2 load	1 C1 load	1 C5 load
Maximum Wiring Capacitance	1000pf	300pf	50pf

NOTE 1: The binary zero output from the GDM1 may vary from —0.5V to +3V. The level depends on the circuit being driven and does not affect the operation of the GDM1.

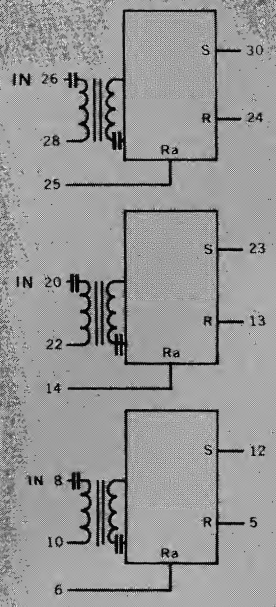
NOTE 2: The GDM1 is suitable for driving one GDI1 or GDI2 Driver Inverter. Because the output voltage level of the GDM1 driving the Inverter is shifted out of tolerance, no other loads should be driven in addition to the GDI1.

PROPAGATION DELAY	10ns	10ns	10ns
POWER REQUIREMENT			
per card			
—12V (pin 32)	34ma	34ma	67ma
+6V (pin 4)	0ma	0ma	0ma
Gnd (pin 18)			

* 8 N loads on Pin 9 and Pin 27

**16 N loads on Pin 9 and Pin 27

GDR1
DATA RECEIVER



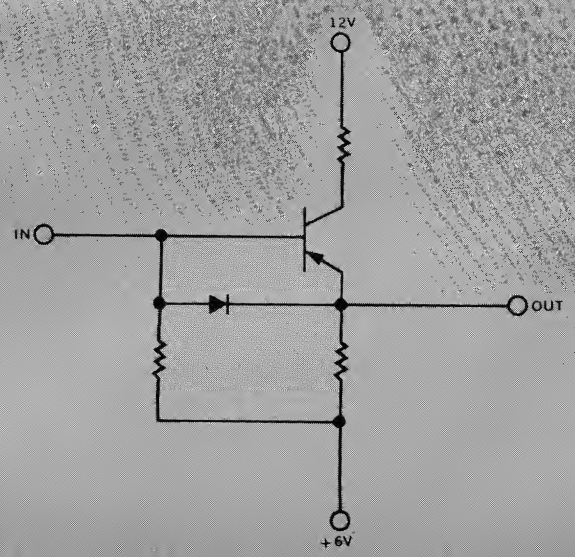
KEY SLOTS PINS 7, 21

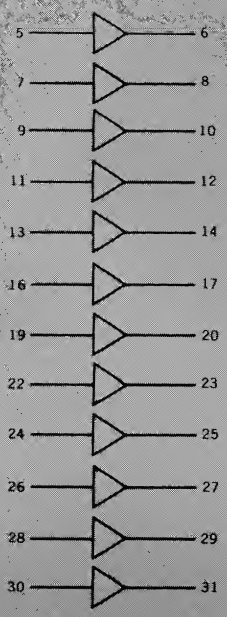
The GDR1 Data Receiver consists of three independent circuits each capable of receiving signals from a cable driven by a GDI2 cable driver. The GDR1 is transformer-coupled at its input and provides ground system and power isolation between transmitter and receiver circuits. Each GDR1 circuit provides "TRUE" (set) and "FALSE" (reset) outputs as well as auxiliary reset input.

The output of the GDR1 is a flip-flop type circuit and may assume either state when power is initially turned on. It may be reset by momentarily grounding the *SET* output through an isolation diode.

SPECIFICATIONS

MODULE	200 KC
DATA RECEIVER	GDR1-.2
INPUT	
Frequency	0 to 200 Kc
Voltage Levels	
One (—10V nominal)	—7 to —12V
Zero (0V nominal)	0.0 to —1V
Max. Rise Time	0.8μsec
OUTPUT	
Voltage Levels (full load)	
One (—10V nominal)	—9 to —10V
Zero (0V nominal)	0.0 to —3V
Max. Rise Time (full load)	55ns
Drive Capability	4 N loads 0 P loads 0 C2 loads
Wiring Capacitance	50pf
POWER REQUIREMENTS	
per card	
—12V (pin 32)	45ma
+6V (pin 4)	3ma
Gnd (pin 18)	





GEF1
EMITTER-FOLLOWER

KEY SLOTS PINS 17, 25

The GEF1 has 12 independent PNP emitter-follower circuits. These are used to provide current gain by offering a high input impedance and low output impedance. In addition, there is a by-pass diode around each emitter-follower. This diode couples positive going signals directly to the load, thus providing push-pull drive capability. This overcomes the disadvantage of straight PNP emitter-followers which have good drive capability for negative going signals but poor drive capability for positive going signals. For capacitive loads (circuits which have a capacitor in series with the input) such as GFF2, GIG1, etc., the drive capability of the GEF1 output is approximately the same as the circuit driving into the GEF1.

The input load of the emitter follower is a function of the number of P type loads on the output.
With no P type loads on the output, the input is effectively 3 P loads (200KC emitter follower). P type loads on the output reflect back to the input at the rate of 30 to 1. For example, if the emitter-follower is driving 30 P type loads, the input load of the 200 KC emitter-follower is effectively 4 P type loads (3 + 1).

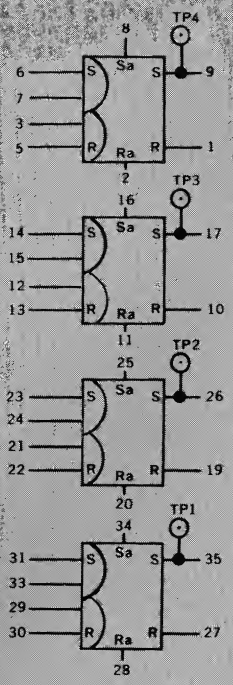
SPECIFICATIONS

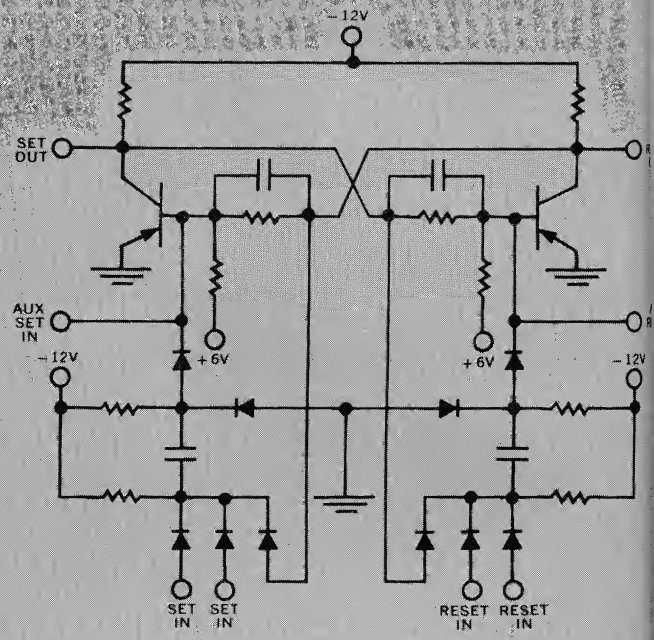
MODULE	200 KC	1 MC	5 MC
EMITTER FOLLOWER	**GEF1-.2**	**GEF1-1**	**GEF1-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One	−9.5 to −12V	−8.5 to −12V	−7.5 to −12V
Zero	+.5 to −1V	+.5 to −1V	+.5 to −1V
Maximum rise time	1μs	0.25μs	60ns
Input Load	3 P loads	4 P loads	8 P loads
OUTPUT			
Voltage Levels (full load)			
One	−9 to −12V	−8 to −12V	−7 to −12V
Zero	+.5 to −.25V	+.5 to −.3V	+.5 to −.3V
Maximum rise time	Same as input signal	Same as input signal	Same as input signal
Maximum fall time	Same as input signal	Same as input signal	Same as input signal
Drive capability	2 N loads 100 P loads C2 loads*	2 N loads 100 P loads C1 loads*	2 N loads 100 P loads C5 loads*
Maximum wiring capacitance	1000pf	500pf	100pf
PROPAGATION DELAY (maximum)	100ns	40ns	15ns
POWER REQUIREMENTS			
per card			
−12V (pin 32)	180ma	200ma	240ma
+6V (pin 4)	180ma	200ma	240ma
Gnd (pin 18)			

*The capability of the GEF1 Emitter-Follower for driving capacitive loads is the same as the circuit driving the Emitter-Follower.

GFF1
UNIVERSAL
FLIP-FLOP

KEY SLOTS PINS 5, 7





The GFF1 has four identical gated flip-flops designed for universal application. Both Set and Reset inputs are controlled by 3 input DC AND gates. One input to each gate is internally connected to the flip-flop output to form a J-K type flip-flop. The circuit is triggered by the trailing edge (positive going edge) of a negative pulse. When all inputs of the gate are at binary one (or left open) the circuit is triggered when one of the inputs rises to binary zero.

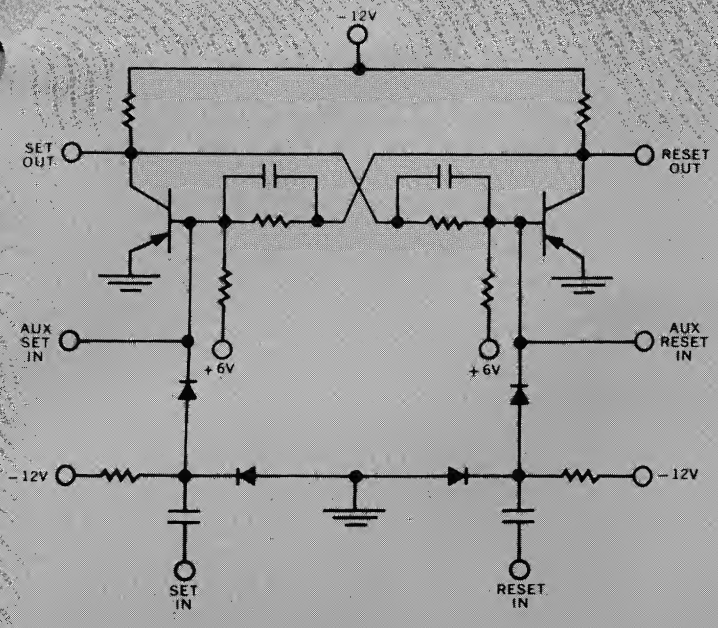
This circuit can be used in the following ways:

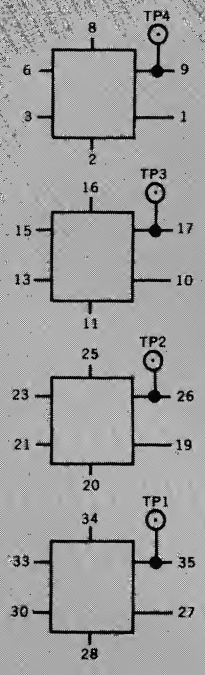
1. As a trigger or binary flip-flop apply pulses to both Set and Reset inputs simultaneously. The circuit will change state with each pulse providing an output frequency of one-half the input frequency.
2. As a Set, Reset flip-flop a pulse applied to the Set input will cause the Set output to go to the binary one state. Once the circuit is in the Set state, subsequent Set pulses have no effect. A pulse applied to the Reset input will cause the Reset output to go to the binary one state.
3. As a serial in and out Shift Register flip-flop, connect the Set output of the first flip-flop to one of the Set inputs of the second flip-flop. Connect the Reset output of the first flip-flop to one of the Reset inputs of the second flip-flop. Connect the unused Set and Reset inputs together and use as a Shift pulse input.

Set and Reset auxiliary inputs are provided and may be operated from input gate (GIG1) or reset gate (GRG1). Since the auxiliary input goes directly to the transistor base, the input gate should be located as close as possible to the flip-flop.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
FLIP-FLOP, UNIVERSAL	**GFF1-.2**	**GFF1-1**	**GFF1-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (−10V nominal)	−9 to −12V	−8 to −12V	−7 to −12
Zero (0V nominal)	+1 to −1V	+1 to −1V	+1 to −1
Clock or Trigger			
Min. Amplitude	8V	8V	7V
Min. dwell at binary one level	2μs	0.4μs	80ns
Maximum rise time	1μs	0.25μs	60ns
Input Load	1 N load	1 N load	2 N loads
Max. number of auxiliary OR inputs per side	7	7	7
Noise Rejection Min. positive noise input for output disturbance of less than 0.5V	2V	2V	1.5V
OUTPUT			
Voltage (Full Load)			
One (−10V nominal)	−9 to −12V	−8 to −12V	−7 to −12
Zero (0V nominal)	0 to −0.25V	0 to −0.3V	0 to −0.3
Maximum rise time (no load)	0.25μs	0.1μs	30ns
Maximum fall time (no load)	0.5μs	0.2μs	50ns
Maximum rise time (full load)	1.0μs	0.25μs	50ns
Drive Capability	9 N loads 5 P loads 2 C2 loads	8 N loads 10 P loads 2 C1 loads	12 N loads 18 P loads 1 C5 load
Maximum Wiring Capacitance per output	1000pf	300pf	50pf
PROPAGATION DELAY From 10% of rising trigger to 10% of rising output (full load)	0.2μs	0.1μs	60ns
POWER REQUIREMENTS per card			
−12V (pin 32)	67ma	80ma	110ma
+6V (pin 4)	1.8ma	1.5ma	2.0ma
Gnd (pin 18)			





GFF2

FLIP-FLOP

RS

KEY SLOTS PINS 17, 21

The GFF2 has four identical AC coupled RS Flip-Flops. A pulse applied to the Set input will cause the Set output to go to the binary one state. Once the circuit is in the Set state, subsequent Set pulses have no effect. A pulse applied to the Reset input will cause the Reset output to go to the binary one state.

The Set, Reset inputs are capacitively coupled and will respond to any positive going level shift having the required amplitude and rise time.

Set and Reset auxiliary inputs provide an alternate path for setting and resetting the circuits through Input Gate GIG1 or Reset Gate GRG1.

The GFF2 may be used as an inexpensive control flip-flop or storage register. It should not be used as a T flip-flop without steered gating.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
FLIP-FLOP, RS	**GFF2-.2**	**GFF2-1**	**GFF2-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (—10V nominal)	—9 to —12V	—8 to —12V	—7 to —12V
Zero (0V nominal)	+1 to —1V	+1 to —1V	+1 to —1V
Clock or Trigger			
Min. Amplitude	8V	8V	7V
Min. dwell at binary one level	2μs	0.4μs	80ns
Maximum rise time	1μs	0.25μs	60ns
Input Load	1 C2 load	1 C1 load	1 C5 load
Max. number of auxiliary OR inputs per side	7	7	7
Noise Rejection Min. positive noise input for output disturbance of less than 0.5V	2V	2V	1.5V
OUTPUT			
Voltage (Full Load)			
One (—10V nominal)	—9 to —12V	—8 to —12V	—7 to —12V
Zero (0V nominal)	0 to —0.25V	0 to —0.3V	0 to —0.3V
Maximum rise time (no load)	0.25μs	0.1μs	30ns
Maximum fall time (no load)	0.5μs	0.2μs	50ns
Maximum rise time (full load)	1.0μs	0.25μs	50ns
Drive capability	10 N loads 5 P loads 2 C2 loads	9 N loads 10 P loads 2 C1 loads	14 N loads 18 P loads 1 C5 load
Maximum wiring capacitance per output	1000pf	300pf	50pf
PROPAGATION DELAY From 10% of rising trigger to 10% of rising output (full load)	0.2μs	0.1μs	60ns
POWER REQUIREMENTS			
per card			
—12V (pin 32)	60ma	65ma	75ma
+6V (pin 4)	1.8ma	1.5ma	2.0ma
Gnd (pin 18)			

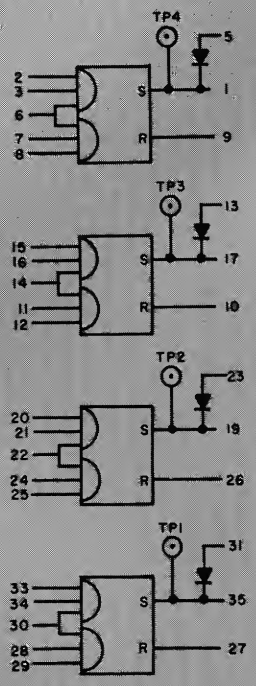
GFF3
UNIVERSAL FLIP-FLOP

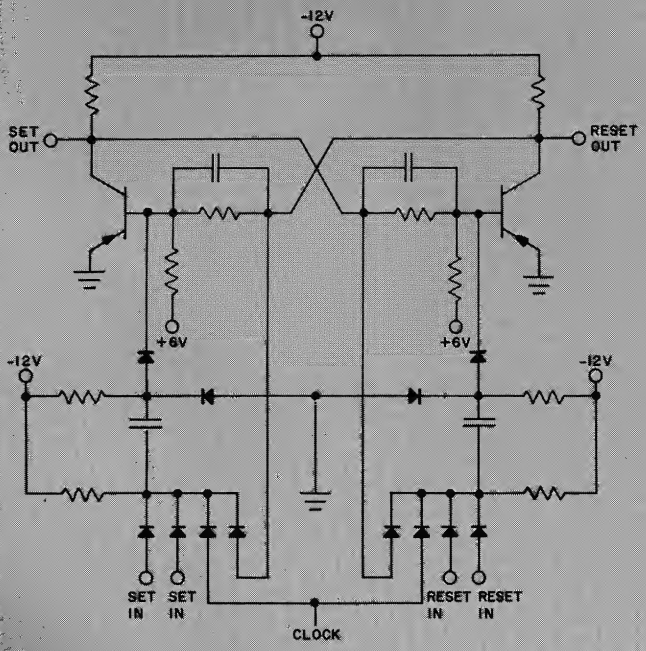
KEY SLOTS PINS 5, 11

The GFF3 contains four identical and independent Eccles-Jordan flip-flop circuits. Each flip flop is provided with Set and Reset diode gates internally cross-connected to the outputs of the flip-flop to perform counting and other basic logic functions. The GFF3 may be externally connected to form a shift register, a binary counter, or a decade counter.

The circuit is triggered by the trailing edge (positive going signal) of a negative pulse.

A collector reset diode is provided at the Set output of each flip-flop. A false level (0V) nominal applied at the collector reset diode will cause the Reset output to go to the true level (−10V nominal).





SPECIFICATIONS

	200 KC	1 MC	5 MC
FLIP-FLOP, UNIVERSAL	GFF3-.2	GFF3-1	GFF3-5
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (−10V nominal)	−9 to −12V	−8 to −12V	−7 to −1
Zero (0V nominal)	+1 to −1V	+1 to −1V	+1 to −
Clock or Trigger			
Min. Amplitude	8V	8V	7V
Min. dwell at binary one level	2μs	0.4μs	80ns
Maximum rise time	1μs	0.25μs	60ns
Gate Input Load	1 N	1 N	2 N
Clock Input Load	2 N	2 N	4 N
Noise Rejection	2V	2V	1.5V
Min. positive noise input for output disturbance of less than 0.5V			
OUTPUT			
Voltage (Full Load)			
One (−10V nominal)	−9 to −12V	−8 to −12V	−7 to −1
Zero (0V nominal)	0 to −0.25V	0 to −0.3V	0 to −0.3
Maximum rise time (no load)	0.25μs	0.1μs	30ns
Maximum fall time (no load)	0.5μs	0.2μs	50ns
Maximum rise time (full load)	1.0μs	0.25μs	50ns
Drive Capability	9 N loads 5 P loads 2 C2 loads	8 N loads 10 P loads 2 C1 loads	12 N loads 18 P loads 1 C5 load
Maximum Wiring Capacitance per output	1000pf	300pf	50pf
PROPAGATION DELAY From 10% of rising trigger to 10% of rising output (full load)	0.2μs	0.1μs	60ns
POWER REQUIREMENTS			
per card			
−12V (pin 32)	67ma	80ma	110ma
+6V (pin 4)	1.8ma	1.5ma	2.0ma
Gnd (pin 18)			

GHA1

HALF ADDER
SUBTRACTOR
COMPARATOR
PARITY
GENERATOR

KEY SLOTS PINS 23, 29

The GHA1 consists of 4 Half Adders or Exclusive Or Gates, 2 Or Gates and 1 And Gate. By use of external jumpers 2 Full Adders, 2 Full Subtractors, or a Parallel Comparator may be implemented. See application section of this specification for proper pin connections.

A Half Adder or Exclusive Or Gate is used to add 2 binary numbers (x and y) to produce output signals representing the sum and carry digits.

Boolean Equation

$$\text{Sum} = x\bar{y} + \bar{x}y$$
$$\text{Carry} = xy$$

A Full Adder is used to add 3 numbers (x, y and c) to produce output signals representing the sum and carry digits. This is accomplished by interconnecting 2 Half Adders and an Or Gate.

Boolean Equation

$$\text{Sum} = x\bar{y}\bar{c} + \bar{x}y\bar{c} + \bar{x}\bar{y}c + x\,y\,c$$
$$\text{Carry} = xy + x\bar{y}c + \bar{x}\,y\,c$$

A Full Subtractor accepts 3 binary numbers (x, y and b) to produce output signals representing the difference (x minus y) and borrow digits. This is accomplished by interconnecting 2 Half Adders and an Or Gate.

Boolean Equation

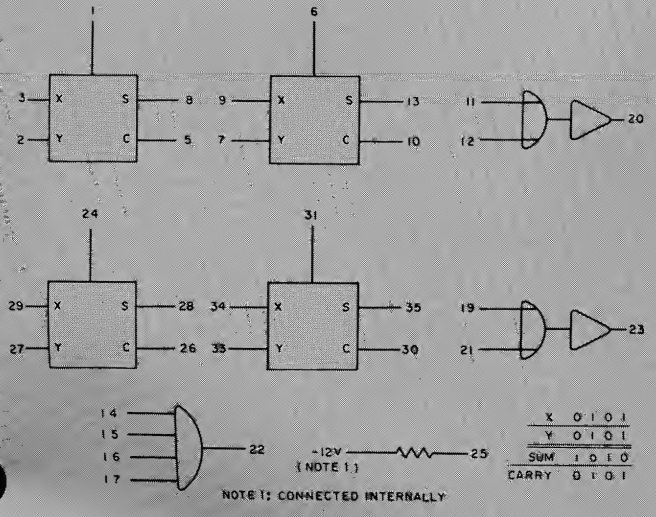
$$\text{Difference} = x\bar{y}\bar{b} + \bar{x}y\bar{b} + \bar{x}\bar{y}b + x\,y\,b$$
$$\text{Borrow} = x\,y\,b + \bar{x}\bar{y}b + \bar{x}y$$

The Parallel Comparator is used to compare 2 binary numbers (x and y) in parallel fashion to produce an output signal when both x and y are alike. Connect $\bar{x}$ and y to Half Adder.

Boolean Equation

$$\text{Output} = (x_1\,y_1 + \bar{x}_1\,\bar{y}_1)\,(\ldots\ldots)\,(x_n\,y_n + \bar{x}_n\,\bar{y}_n)$$

The Half Adder circuit is useful as a parity generator. A minimum of connections are necessary. For n bits n-1 Half Adder circuits are required.

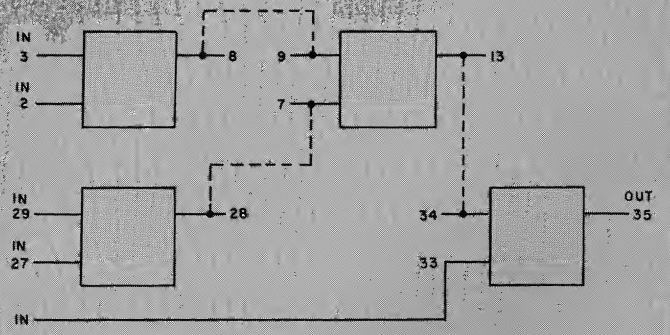


GHA1 QUADRUPLE HALF ADDER

SPECIFICATIONS

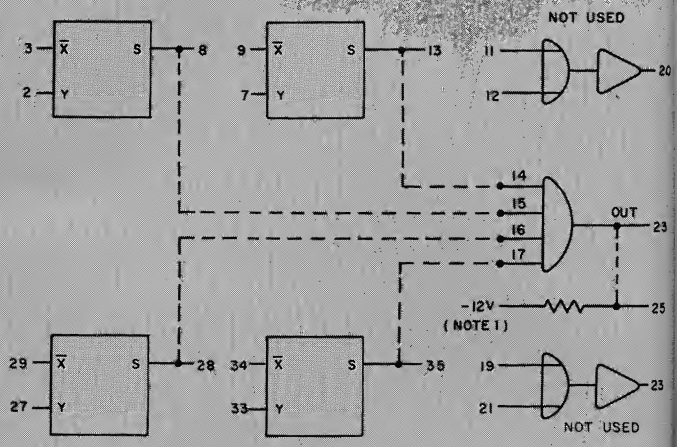
	200KC	1MC	5MC
HALF ADDER	**GHA1-2**	**GHA1-1**	**GHA1-5**
INPUT (Pins 2, 3, 7, 9, 27, 29, 33 & 34):			
Frequency	0 to 200KC	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (nominal —10V)	—9 to —12V	—8 to —12V	—7 to —12V
Zero (nominal 0V)	—1 to 1V	—1 to 1V	—1 to 1V
Max Rise Time	2.5μs	0.4μs	100ns
Max Fall Time	2.5μs	0.4μs	100ns
Input Load	6 P loads 2 N loads	6 P loads 2 N loads	6 P loads 2 N loads
Noise Rejection Min. noise input for output disturbance less than 2.0 volts.	1.5V	1.5V	1.5V
OUTPUT (Pins 8, 13, 28 & 35):			
Voltage (Full Load)			
One (nominal —10V)	—9 to —12V	—8 to —12V	—7 to —12V
Zero (nominal 0V)	0 to —.5V	0 to —.5V	0 to —.5V
Max Rise Time (No load)	.3μs	.1μs	40ns
Max Rise Time (Full load)	1.0μs	.25μs	60ns
Max Fall Time (No load)	.5μs	.2μs	100ns
Max Drive Capability	15 N loads 12 P loads 4 C2 loads	8 N loads 8 P loads 4 C1 loads	10 N loads 20 P loads 2 C5 loads
Max Wiring Capacitance	1000pf	300pf	50pf
Propagation Delay	0.3μs	0.1μs	50μs
Or Gate			
INPUT (Pins 11, 12, 19 & 21):			
Frequency	0 to 200 KC	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (Nominal —10V)	—9 to —12V	—8 to —12V	—7 to —12V
Zero (Nominal 0V)	—1 to 1V	—1 to 1V	—1 to 1V
Max Rise Time	2.5μs	0.4μs	100ns
Max Fall Time	2.5μs	0.4μs	100ns
Input Load	2 P loads	3 P loads	4 P loads
OUTPUT (Pins 20 & 23):			
Voltage Levels			
One	—9 to —12V	—8 to —12V	—7 to —12V
Zero	0 to —.5V	0 to —.5V	0 to —.5V
Max Rise Time (No load)	0.3μs	0.1μs	40ns
Max Rise Time (Full load)	1.0μs	0.25μs	60ns
Max Fall Time (No load)	0.5μs	0.1μs	100ns
Drive Capability	15 N loads 10 P loads 4 C2 loads	10 N loads 12 P loads 4 C1 loads	15 N loads 15 P loads 4 C5 loads
Max Wiring Capacitance	1000pf	300pf	50pf
Propagation Delay	0.2μs	0.1μs	50ns
And Gate (Same as GDG2-1)			
Power Requirements (per card)			
—12VDC (pin 32)	145ma	168ma	174ma
+6VDC (pin 4)	2.6ma	4.0ma	4.4ma
Gnd (pin 18)			

GHA1 APPLICATIONS



OUTPUT IS BINARY "1" WHEN ODD NUMBER OF INPUTS ARE BINARY 1.

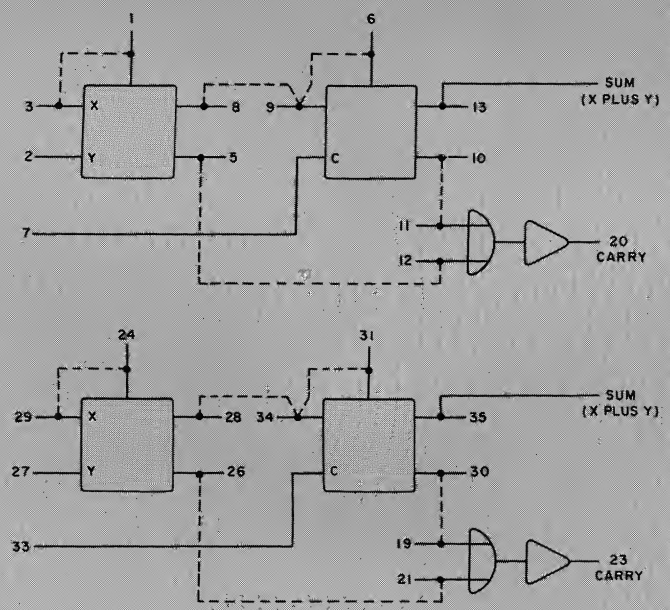
GHA1 PARITY GENERATOR, 5 BIT



NOTE: 1. CONNECTED INTERNALLY
2. DASH LINES ARE EXTERNAL JUMPERS

	n			
	1	2	3	4
X	0	0	1	0
Y	0	0	1	0
OUT	1	1	1	1

GHA1 PARALLEL COMPARATOR

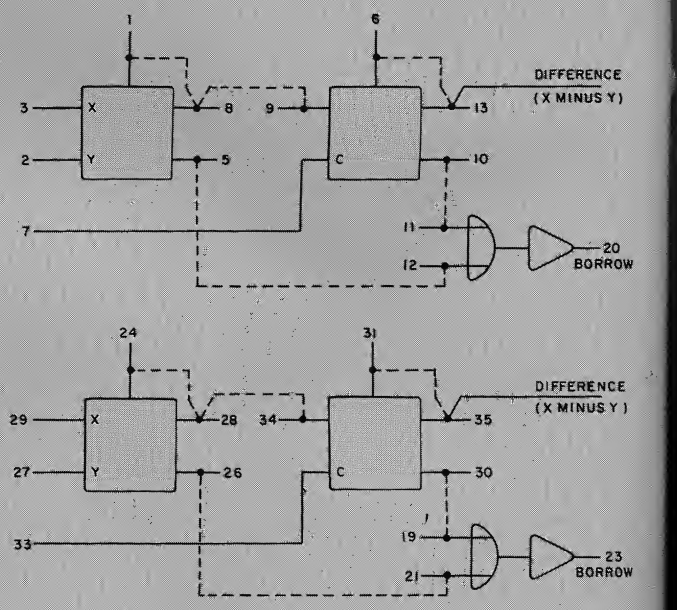


NOTE: 1. CONNECTED INTERNALLY
2. DASH LINES ARE EXTERNAL JUMPERS

EXAMPLE

	8	4	2	1	
X	0	1	1	1	7
Y	0	1	1	0	6
SUM	1	1	0	1	13
CARRY					

GHA1 DUAL FULL ADDER



NOTES: 1. CONNECTED INTERNALLY.
2. DASH LINES ARE EXTERNAL JUMPERS.

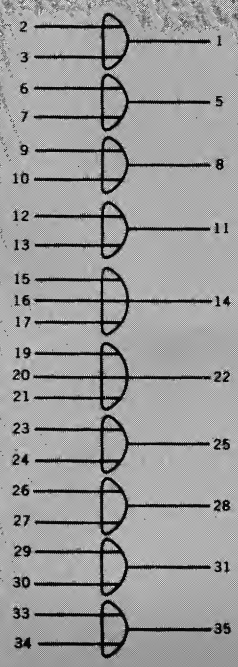
EXAMPLE

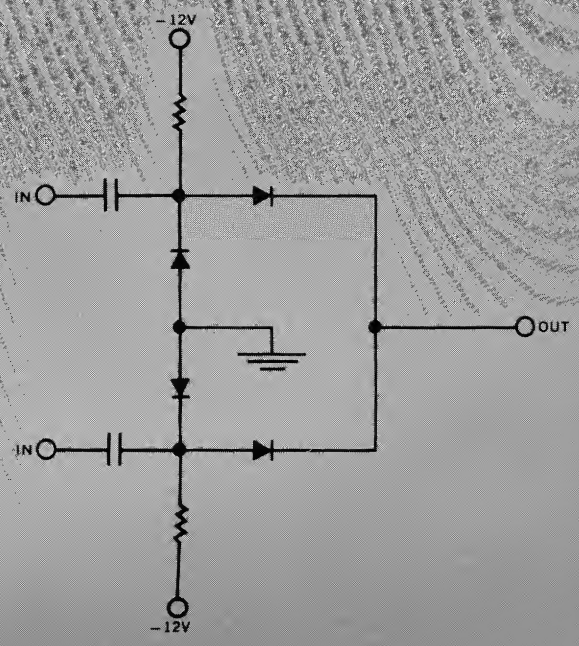
	8	4	2	1	
X	1	0	1	0	10
Y	0	1	1	0	-6
DIFFERENCE	0	1	0	0	4
BORROW					

GHA1 DUAL FULL SUBTRACTOR

GIG1
INPUT GATE

KEY SLOTS PINS 5, 19





The GIG1 has eight two-input and two three-input AC coupled OR Gates. These gates are connected to the *auxiliary* input of flip-flops to provide alternate trigger sources. When a positive going level shift with the proper amplitude and rise time is applied to any one of the gate inputs, a pulse is coupled through to trigger the flip-flop. The gates may be expanded simply by connecting the outputs of two or more gates together. Up to 7 inputs may be connected to a flip-flop.

NOTE: The auxiliary input to the flip-flop is connected directly to the transistor base. Since this is a relatively sensitive point, the input gate should be located close to the flip-flop being driven.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
INPUT GATE	**GIG1-.2**	**GIG1-1**	**GIG1-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (nominal −10V)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (nominal 0V)	+1 to −1V	+1 to −1V	+1 to −1V
Minimum Amplitude	8V	8V	7V
Minimum dwell at binary one level	2μs	0.4μs	80ns
Maximum rise time	1μs	0.25μs	60ns
Input Load	1 C2 load	1 C1 load	1 C5 load
Noise Rejection	2.0V	2.0V	1.5V
OUTPUT			
Voltage Levels (full load)			
Input rising to gnd.	+7 to +12V	+6 to +12V	+5 to +12V
Steady state	0 to −1.0V	0 to −1.0V	0 to −1.0V
Maximum rise time	Same as input	Same as input	Same as input
Maximum loading			
Flip-Flop (Aux. input)	1	1	1
Maximum wiring capacitance	200pf (very critical)	75pf (very critical)	20pf (very critical)
PROPAGATION DELAY	10ns	10ns	10ns
POWER REQUIREMENTS			
per card			
−12V (pin 32)	6.5ma	10ma	16ma
+6V (pin 4)	0	0	0
Gnd (pin 18)			

GLA1-1
LINEAR AMPLIFIER

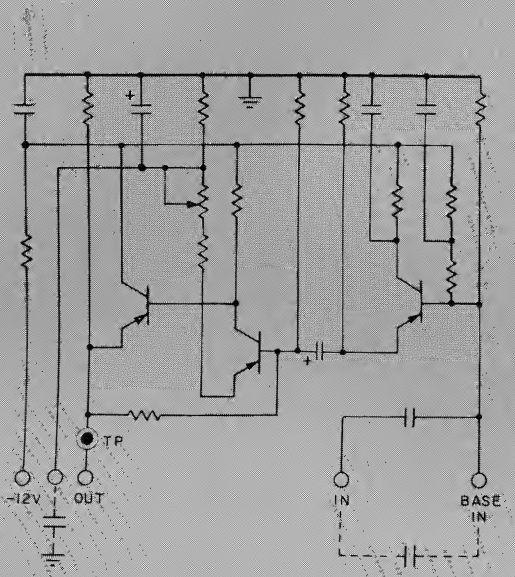
KEY SLOTS PINS 23, 31

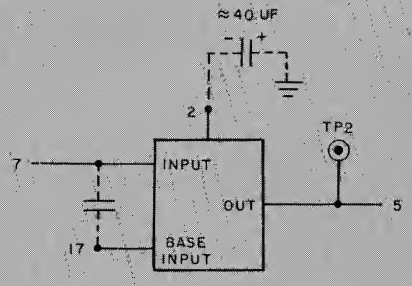
The GLA1-1 Germanium digital module consists of 2 linear amplifier circuits used for detection of small input signals. Input signals may be sine waves, square waves or pulses. Frequency response of this circuit is from 20 cps to 1 mc, depending on gain. A gain adjustment control is provided so that output gains may be adjusted from 10 to 90 as required.

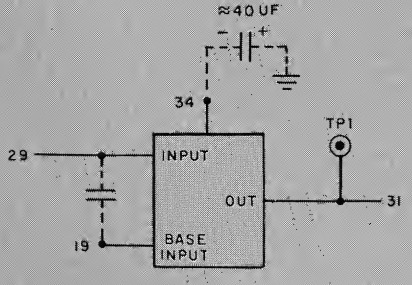
A direct base input pin is provided so that a large capacitor may be added to extend the low frequency range.

Input-output signals are inverted (180° out of phase).

To extend the low frequency range external capacitors may be connected as shown by the dotted lines in the schematic.





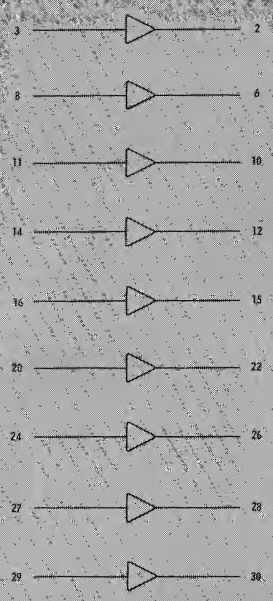


SPECIFICATIONS

LINEAR AMPLIFIER	GLA1-1
INPUT:	
Frequency (Sine Wave)	20cps to 1Mc
Max. Voltage	12V PP
Min. Voltage	5MV
Impedance	50K @ 20cps 20K @ 1Kc 20K @ 10Kc 10K @ 100Kc 5K @ 1Mc
OUTPUT:	
Amplitude (for linear operation peak to peak)	6V
Voltage (Gain adjust)	10 to 90
D.C. Level (Nominal)	—7V
Phase Shift	180 Degrees
Impedance	1KΩ
Random Output Noise	20MV
Drive Capability	1 GST2-2, —1 or —5 (cap. input) or 1 GLA1-1
Gain Stability (Typ.)	
@ Gain=10	.5%
@ Gain=90	2.0%
POWER REQUIREMENTS (per card):	
—12VDC (pin 32) Gnd (pin 18)	6ma

GLC1-.2
LEVEL CONVERTER

KEY SLOTS PINS 7, 29



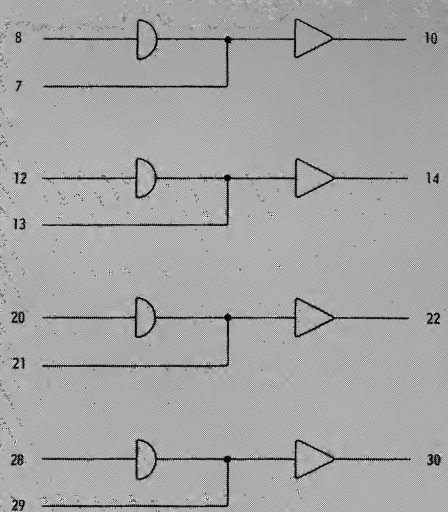
The GLC1 consists of nine identical and independent circuits capable of converting positive voltage signals to negative voltage signals. The GLC1 will also convert voltage mode IBM 7090 or 7094 logic levels (0 V = false, −10 V = true). A binary ONE positive voltage in, will cause a binary ONE negative voltage out.

SPECIFICATIONS

MODULE	200 KC
LEVEL CONVERTER	**GLC1-.2**
INPUT:	
Frequency	0 to 200Kc
Voltage Levels	
One (nominal +8V)	+6 to +12V
Zero (nominal 0V)	−1 to +1V
Current	
One	+3ma
Zero	0ma
Max. Rise Time	1.2μs
Max. Fall Time	1.2μs
OUTPUT:	
Voltage Levels	
One (nominal −10V)	−9 to −12V
Zero (nominal 0V)	0 to −.5V
Rise Time (No load)	0.25μs
Fall Time (No load)	0.5μs
Rise Time (Full load)	0.8μs
Drive Capability	8 N loads 9 P loads 5 C2 loads
Wiring Capacitance	1000 pf
PROPAGATION DELAY	0.2μs
POWER REQUIREMENT (per card):	
−12 VDC (pin 32)	88ma
+6 VDC (pin 4)	None
Gnd (pin 18)	

GLC2-.2
LEVEL CONVERTER

KEY SLOTS PINS 7, 31



A binary ONE (−10V) in will cause a binary ZERO (0V) output.

The GLC2 consists of four identical and independent circuits capable of converting negative voltage levels to positive voltage levels. The GLC2 will also convert standard Raytheon logic levels to voltage mode IBM 7090 logic levels.

Each circuit will drive 150 feet of coaxial cable.

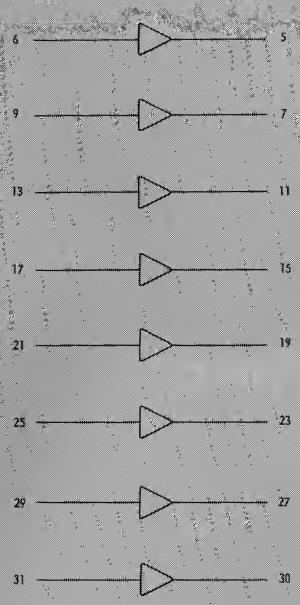
Auxiliary inputs are made available for each circuit to extend gating of input signals.

SPECIFICATIONS

MODULE	200 KC
LEVEL CONVERTER	**GLC2-.2**
INPUT:	
Frequency	0 to 200Kc
Voltage Levels	
One (nominal −10V)	−7 to −12V
Zero (nominal 0V)	0 to −1V
Max. Rise Time	1.0μs
Max. Fall Time	1.8μs
Load	2N
OUTPUT:	
Voltage Levels	
One (nominal +10V)	+6 to +11V
Zero (nominal 0V)	0 to 1.5V
Rise Time (No load)	0.2μs
Fall Time (Full load)	1.8μs
Rise Time (Full load)	0.8μs
Drive Capability	100ma returned to gnd or +12V or 150 feet RG-62B/U Terminated with 93Ω
Wiring Capacitance	200 pf
PROPAGATION DELAY	0.3μs
POWER REQUIREMENT (per card):	
−12 VDC (pin 32)	20ma
+12 VDC (pin 6)	500ma
Gnd (pin 18)	

GLC3-.2
LEVEL CONVERTER

KEY SLOTS PINS 11, 13



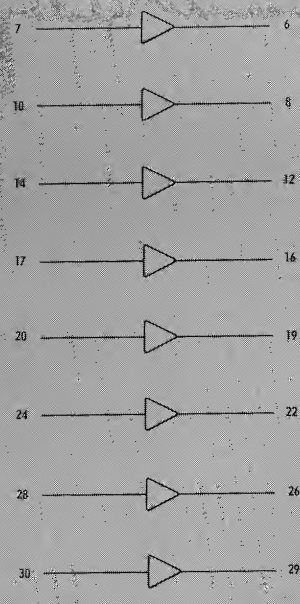
The GLC3-.2 consists of eight identical and independent circuits capable of converting Raytheon 200kc logic levels into IBM current mode "P" levels. Each GLC3-.2 circuit is designed to drive 25 feet of coaxial cable and provide specified output at the other end of the cable.

SPECIFICATIONS

MODULE	200 KC
LEVEL CONVERTER	**GLC3-.2**
INPUT:	
Frequency	0-200Kc
Voltage Levels	
One (nominal −10V)	−8 to −12V
Zero (nominal 0V)	+1.0 to −1.0V
Max. Rise Time	1μs
Input Load	12 P loads 1 C2 load
OUTPUT:	
Voltage Levels (Full load)	
One	−3.2 to −5.5V
Zero	−6.6 to −9.2V
Max. Rise Time (No load)	−0.2μs
Max. Fall Time (Full load)	−1.2μs
Max. Rise Time (Full load)	−0.6μs
Drive Capability	25 ft. of coaxial cable to IBM "P" load
Max. Wiring Capacitance	400 pf
PROPAGATION DELAY	0.2μs
POWER REQUIREMENTS (per card):	
−12V (pin 32)	64ma max.
+6V (pin 4)	5ma max.
Gnd (pin 18)	

GLC4-.2
LEVEL CONVERTER

KEY SLOTS PINS 9, 33



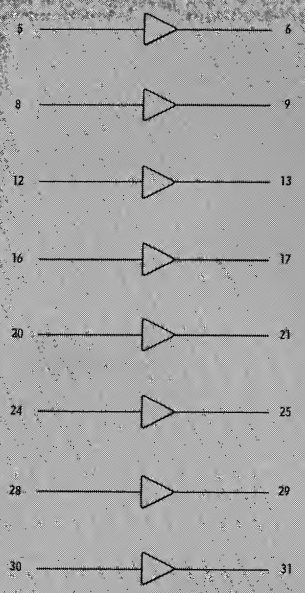
The GLC4-.2 consists of eight identical and independent circuits capable of converting Raytheon 200kc logic levels into IBM current mode N levels. Each GLC4-.2 circuit will drive 25 feet of coaxial cable into a GLC5-.2 or an IBM N Line Terminator. A Binary ONE (−10 V) in will provide +N out.

SPECIFICATIONS

MODULE	200 KC
LEVEL CONVERTER	**GLC4-.2**
INPUT:	
Frequency	0-200Kc
Voltage Levels	
One (nominal −10V)	−8 to −12V
Zero (nominal 0V)	+1.0 to −1.0V
Max. Rise Time	1μs
Input Load	12 P loads 1 C2 load
OUTPUT:	
Voltage Levels (Full load)	
One (+N)	+0.5 to +1.3V
Zero (−N)	−0.5 to −2.4V
Max. Rise Time (No load)	−0.2μs
Max. Fall Time (Full load)	−1.2μs
Max. Rise Time (Full load)	−0.8μs
Drive Capability	25 ft. of coaxial cable to IBM "N" load
Max. Wiring Capacitance	400 pf
PROPAGATION DELAY	0.2μs
POWER REQUIREMENTS (per card):	
−12V (pin 32)	64ma max.
+6V (pin 4)	55ma max.
Gnd (pin 18)	

GLC5-.2
LEVEL CONVERTER

KEY SLOTS PINS 11, 17



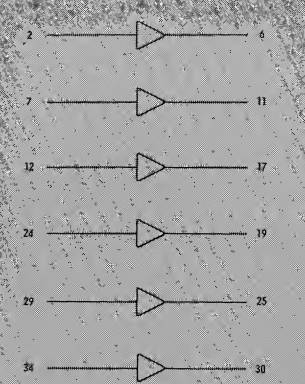
The GLC5-.2 consists of eight identical and independent circuits capable of converting IBM current mode "N" levels to Raytheon 200 KC logic levels. IBM "N" level inputs can be accepted through a coaxial cable up to 25 feet long driven by an IBM N Line Driver. A +N signal into the GLC5 will provide a binary ONE (—10 V) out.

SPECIFICATIONS

MODULE	200 KC
LEVEL CONVERTER	**GLC5-.2**
INPUT:	
Frequency	0 to 200Kc
Voltage Levels	
One (+N)	+0.2 to +1.0V
Zero (—N)	—0.2 to —1.0V
Current	
One	+6ma
Zero	—0.1ma
Max. Rise Time	0.8μs
Max. Fall Time	0.8μs
OUTPUT:	
Voltage Levels	
One (nominal —10V)	—9 to —12V
Zero (nominal 0V)	0 to —0.5V
Max. Rise Time (No load)	0.2μs
Max. Fall Time (No load)	0.5μs
Max. Rise Time (Full load)	0.8μs
Drive Capability	8 N loads 8 P loads 4 C2 loads
Max. Wiring Capacitance	1000 pf
PROPAGATION DELAY (Typical):	0.2μs
POWER REQUIREMENTS (per card):	
—12V (pin 32)	76ma max.
+6V (pin 4)	None
Gnd (pin 18)	

GLC6-.2
LEVEL CONVERTER

KEY SLOTS PINS 11, 15



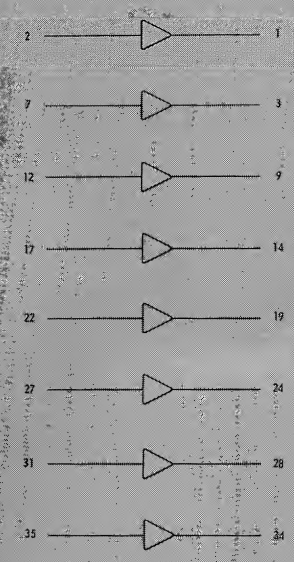
The GLC6-.2 consists of six identical and independent circuits capable of converting IBM current mode "P" levels to Raytheon 200 KC logic levels. IBM "P" level inputs can be accepted through a coaxial cable up to 25 feet long.

SPECIFICATIONS

MODULE	200 KC
LEVEL CONVERTER	**GLC6-.2**
INPUT:	
Frequency	0 to 200Kc
Voltage Level	
One	—6.4 to —9V
Zero	—3 to —5.4V
Current	
One	+0.1ma
Zero	—6ma
Max. Rise Time	0.8 μs
Max. Fall Time	0.8μs
OUTPUT:	
Voltage (Full load)	
One (nominal —10V)	—9 to —12V
Zero (nominal 0V)	0 to —0.5V
Max. Rise Time (No load)	0.2μs
Max. Fall Time (Full load)	0.8μs
Max. Rise Time (Full load)	0.8μs
Drive Capability	8 N loads 8 P loads 4 C2 loads
Max. Wiring Capacitance	1000 pf
PROPAGATION DELAY (Typical):	0.2μs
POWER REQUIREMENTS (per card):	
—12V (pin 32)	64ma max.
+6V (pin 4)	9ma max.
Gnd (pin 18)	

GLC7-1
LEVEL CONVERTER

KEY SLOTS PINS 13, 19



SPECIFICATIONS

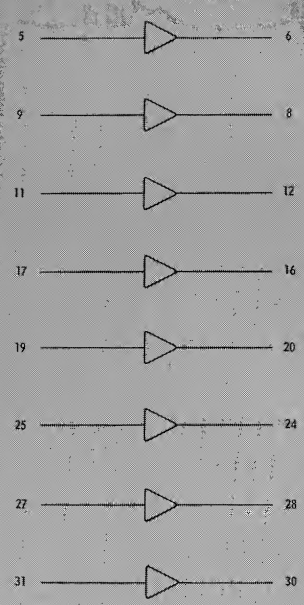
MODULE	1 MC
LEVEL CONVERTER	**GLC7-1**
INPUT:	
"0"	+1 to −1V
"1"	−8 to −12V
Loading	1 N load
Max. rise time	100nsec.
Max. fall time	150nsec.
OUTPUT:	
"+C"	+1V nominal
"−C"	−2V nominal
Rise time	20nsec. max.
Fall time	40nsec. max.
POWER REQUIREMENT:	
−12V (pin 32)	460ma
+6V (pin 4)	20ma
Gnd (pin 18)	

The GLC7-1 module contains eight (8) separate and identical level converter circuits. The circuits convert from Raytheon Computer standard logic levels to IBM "C" levels and are therefore "C" line drivers. The "C" levels are developed in the low impedance (approximately 120 ohms) of a terminator circuit. Appropriate terminators to be used would be the IBM "C Line Terminator" or a Raytheon Computer GLC8-1. The use of a low impedance terminated line allows megacycle data transmission rates without ringing, reflection or overshoot. Since the return current of this line requires a direct ground connection between drivers and terminator, the GLC7-1 is appropriate only where the ground loop created by multiple ground connectors can be tolerated. Recommended cables are 93 ohm coax or twisted pair.

Binary "0" (0v) at the input to the GLC7-1 causes IBM "−C" (−2v) at the output. Binary "1" (−10v) at the input to the GLC7-1 causes IBM "+C" (+1v) at the output.

GLC8-1
LEVEL CONVERTER

KEY SLOTS PINS 13, 21



SPECIFICATIONS

MODULE	1 MC
LEVEL CONVERTER	**GLC8-1**
INPUT:	
"+C"	+1V nominal
"−C"	−2V nominal
Rise Time	50nsec. typical
Fall Time	100nsec. typical
OUTPUT:	
"0"	0 to −.3V
"1"	−8 to −12V
Rise Time	60nsec. typical
Fall Time	30nsec. typical
Drive Capability	8 N loads
	2 P loads
	2 CI loads
POWER REQUIREMENTS:	
−12V (pin 32)	80ma
+6V (pin 4)	110ma
Gnd (pin 18)	

The GLC8-1 module contains eight (8) separate and identical level converter circuits. The circuits convert from IBM "C" levels to Raytheon Computer standard logic levels, and are therefore "C" line terminators.

IBM "−C" (−2v) at the input to the GLC8-1 causes binary "0" (0v) at the output. IBM "+C" (+1v) at the input to the GLC8-1 causes "1." (−10v) at the output.

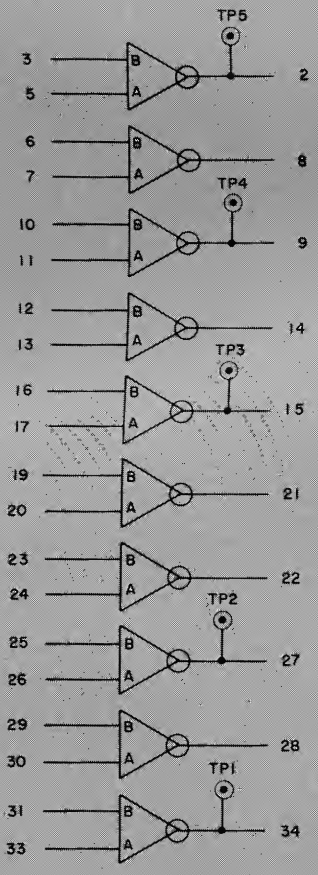
The GLC9 module consists of 10 identical and independent circuits capable of converting low level signals to standard Raytheon Computer levels (0v = false, −10v = true).

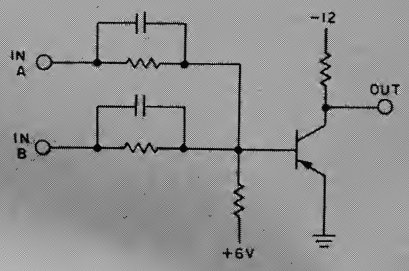
Input "A" converts 0V and −3V to −10V and 0V respectively. Input "B" converts 0V and −6V to −10V and 0V respectively.

Input to output signals are inverted.

GLC9
LEVEL CONVERTER

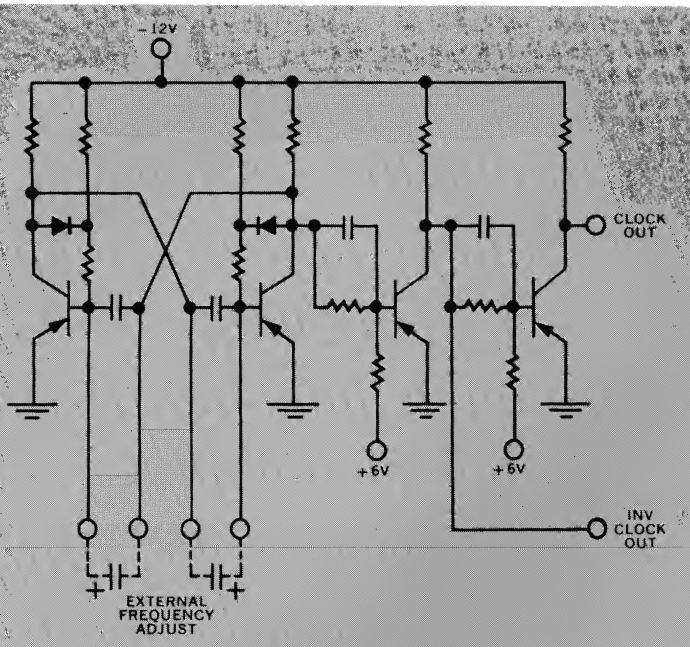
KEY SLOTS PINS 23, 27

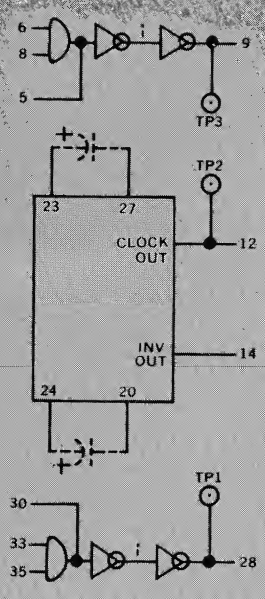




SPECIFICATIONS

LEVEL CONVERTER	GLC9-2	GLC9-1	GLC9-5
INPUT "A"			
Frequency	0 to 200KC	0 to 1MC	0 to 5MC
Voltage Levels			
One	−3 to −12V	−3 to −12V	−3 to −12V
Zero	−.3 to +.3V	−.3 to +.3V	−.3 to +.3V
Maximum Rise Time	2.0μs	.3μs	60ns
Maximum Fall Time	2.0μs	.3μs	60ns
Input Load			
Resistive to GND	2.7KΩ	2.2KΩ	1.8KΩ
Capacitive	47pf	47pf	22pf
Noise Rejection	.7V	.7V	.7V
Min. noise input for output disturbance less than 2.0V.			
INPUT "B"			
Frequency	0 to 200KC	0 to 1MC	0 to 5MC
Voltage Levels			
One	−6 to −12V	−6 to −12V	−6 to −12V
Zero	−.5 to +.5V	−.5 to +.5V	−.5 to +.5V
Maximum Rise Time	2.0μs	.4μs	60ns
Maximum Fall Time	2.0μs	.4μs	60ns
Input Load			
Resistive to GND	3.9KΩ	3.3KΩ	3.0KΩ
Capacitive	330pf	47pf	22pf
Noise Rejection	1.5V	1.5V	1.5V
Min. noise input for output disturbance less than 2.0V.			
OUTPUT			
Voltage Levels (full load)			
One (nominal −10V)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (nominal 0v)	0 to −.3V	0 to −.3V	0 to −.3V
Rise Time (No load)	0.3μs	0.1μs	30ns
(Full load)	1.0μs	0.25μs	60ns
Fall Time (No load)	0.5μs	0.2μs	60ns
Drive Capability (Using Input A)	7N	5N	7N
(Using Input B)	25N	9N	10N
(Using Input A or B)	6P	6P	12P
(Using Input A or B)	4C2	2C1	2C5
Maximum Wiring Capacity	1000pf	500pf	50pf
Propagation Delay	.15μs	60ns	15ns
POWER REQUIREMENTS (per card)			
−12VDC (pin 32)	92ma	117ma	140ma
+6VDC (pin 4)	2.6ma	3.2ma	3.9ma
Gnd (pin 18)			





GMV1
MULTIVIBRATOR CLOCK

KEY SLOTS PINS, 15, 19

The GMV1 is comprised of an astable (free running) multivibrator and two gated drivers.

The nominal frequency of the GMV1-.2 multivibrator is 200KC. The nominal frequency of the GMV1-1 is 1MC. Contacts are provided for external capacitors to obtain lower frequencies. Both the normal and inverted outputs are available. The clock output has an internal amplifier to provide fast rise time and good drive capability.

The gated driver circuits each have a 2 input diode AND Gate followed by a non-inverting drive circuit designed for heavy drive capability. These drivers may be used in conjunction with the multivibrator to provide a gated clock, or they may be used as separate drive circuits.

NOTE: When operating the GMV1 at less than ½ maximum rated frequency, the drive capability for capacitive loads is doubled.

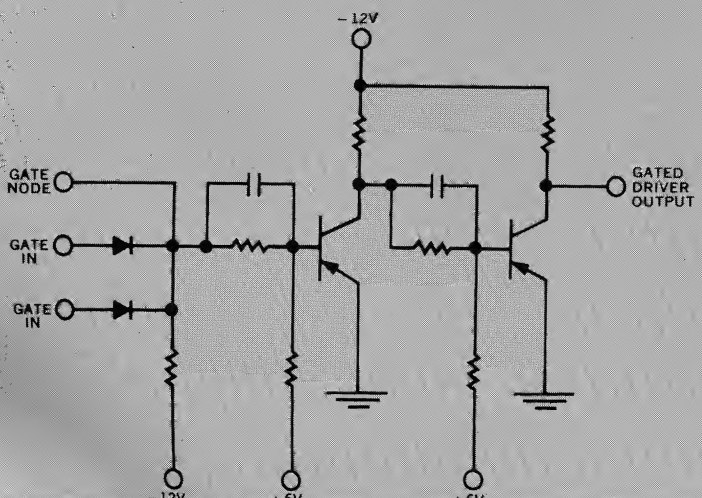
NOTE: The approximate value of the capacitors needed for any given frequency may be found by using the formula:

$$C = 33T$$

where C is timing capacitance in pf

T is period in μs

The minimum frequency is determined primarily by the practical size of available capacitors.



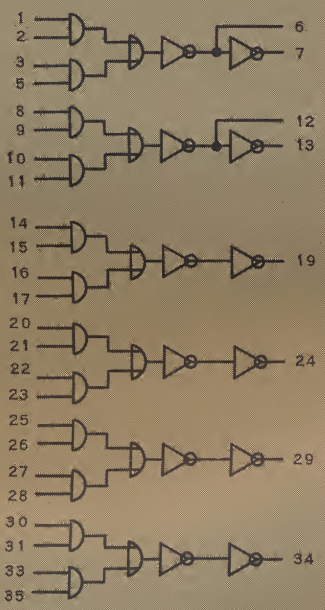
SPECIFICATIONS

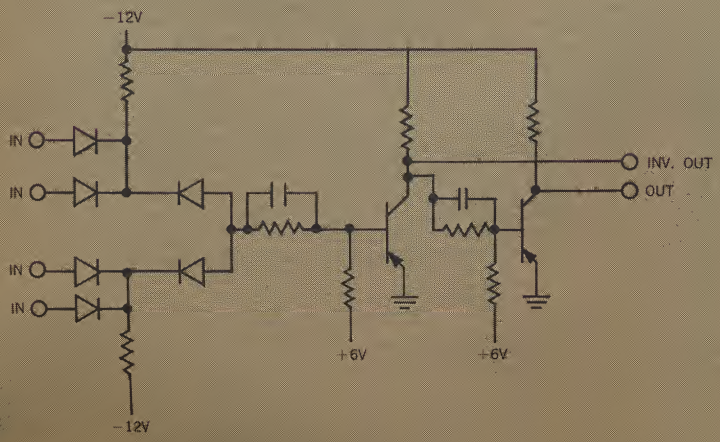
MODULE	200 KC	1 MC	5 MC
MULTIVIBRATOR	GMV1-.2	GMV1-1	
INPUT (Gated Driver)			
Frequency	0 to 200 Kc	0 to 1 Mc	
Voltage Levels			
One (Nominal −10V)	−9 to −12V	−8 to −12V	
Zero (Nominal 0V)	+1 to −1V	+1 to −1V	For 5 Mc adjustable
Maximum Rise Time	2.5μs	0.5μs	clock
Maximum Fall Time	2.5μs	0.5μs	use
Input Load	1 N load	1 N load	GCG1-5
OUTPUT			
Voltage Levels (full load)			
One (Nominal −10V)	−9.5 to −12V	−8.5 to −12V	
Zero (Nominal 0V)	0 to −0.3V	0 to −0.5V	
Maximum Rise Time (no load)	0.25μs	0.1μs	
Maximum Fall Time (no load)	0.5μs	0.2μs	
Maximum Rise Time (full load)	1.0μs	0.25μs	
Drive Capability			
Multivibrator Clock Out	20 N loads 20 P loads 20 C2 loads	10 N loads 25 P loads 10 C1 loads	
Multivibrator Inv Out (Use only above 50 Kc)	1 N load 0 P load 1 C2 load	1 N load 0 P load 1 C1 load	
Gated Driver	50 N loads 20 P loads 8 C2 loads	10 N loads 25 P loads 4 C1 loads	
Maximum Wiring Capacitance	1000pf	300pf	
PROPAGATION DELAY (Gated Driver)	0.4μs	0.2μs	
POWER REQUIREMENTS per card			
−12Vdc (pin 32)	70ma	70ma	
+ 6Vdc (pin 4)	2ma	2ma	
Gnd (pin 18)			

GDG6
DIODE GATE

KEY SLOTS PINS 11, 19

The GDG6 contains six AND/OR gates. Each gate has four inputs and a level-restoring output. Two of the gates have an additional inverting output. Since all outputs restore logic levels, cascading is unlimited in this respect.





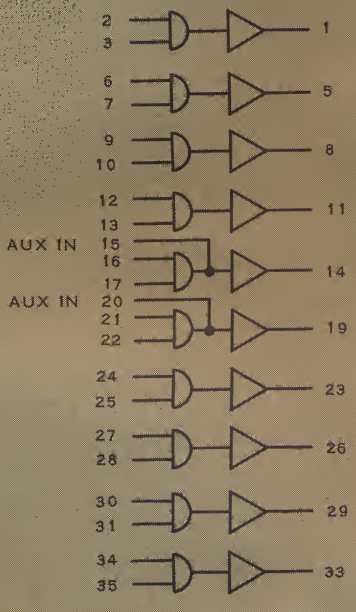
SPECIFICATIONS

MODULE	200 KC
DIODE GATE	GDG6-.2
INPUT	
Frequency	0 to 200 Kc
Voltage Levels	
One (nominal −10V)	−9 to −10V
Zero (nominal 0V)	+1 to −1V
Maximum Rise Time	2.5μs
Input Load	1 N load
OUTPUT	
Voltage Levels (full load)	
One (nominal −10V)	−9 to −12V
Zero (nominal 0V)	0 to −0.3V
Maximum Rise Time (no load)	0.3μs
Maximum Fall Time (no load)	0.3μs
Maximum Rise Time (full load)	0.4μs
Drive Capability	
Output Pins 19, 24, 29, 34 (non-inverted)	30 N loads 10 P loads 4 C2 loads
Output Pins 7, 13 (non-inverted)	7 N loads 6 P loads 2 C2 loads
Output Pins 6, 12 (inverted)	3 N loads 5 P loads 2 C2 loads
Maximum Wiring Capacitance	1000 pf
Noise Rejection	2V
PROPAGATION DELAY	
(in chain of gates between consecutive outputs—full load)	0.3μs
POWER REQUIREMENTS	
−12VDC	140ma
+ 6VDC	10ma

GGD1
GATED DRIVER

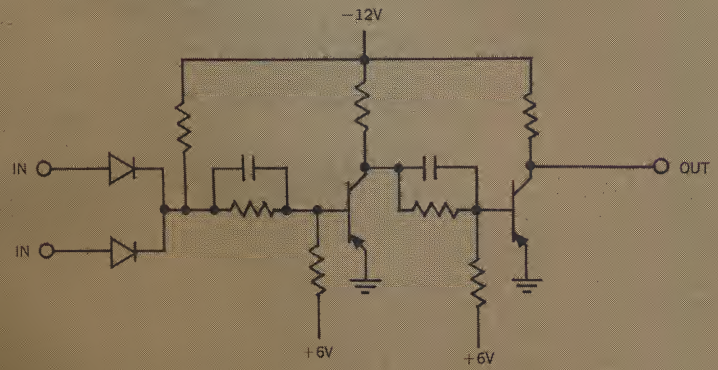
KEY SLOTS PINS 11, 23

The GGD1 contains ten independent gated-driver circuits. Each circuit is a two-input AND gate with a level-restoring driver output. Two of the circuits have the input node brought out to an input pin. Only diode AND gates can be connected to these nodes.



SPECIFICATIONS

MODULE	200 KC
GATED DRIVER	**GGD1-.2**
INPUT	
Frequency	0 to 200 Kc
Voltage Levels	
One (nominal —10V)	—9 to —12V
Zero (nominal 0V)	+1 to —1V
Maximum Rise Time	2.5μs
Input Load	1 N load 1 C2 load
OUTPUT	
Voltage Levels (full load)	
One (nominal —10V)	—9 to —12V
Zero (nominal 0V)	0 to 0.3V
Maximum Rise Time (no load)	0.2μs
Maximum Fall Time (no load)	0.3μs
Maximum Rise Time (full load)	0.3μs
Drive Capability	50 N loads 16 P loads 4 C2 Loads
Maximum Wiring Capacitance	1000 pf
PROPAGATION DELAY (full load — in chain of gates between consecutive outputs.)	0.5μs
NOISE REJECTION	2V
POWER REQUIREMENTS	
Per Card	
—12VDC	310ma
+ 6VDC	15.5ma



GSR4
SHIFT REGISTER

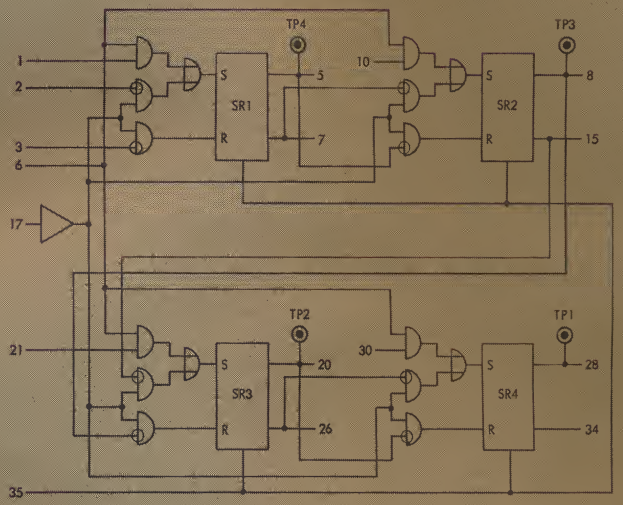
KEY SLOTS PINS 23, 33

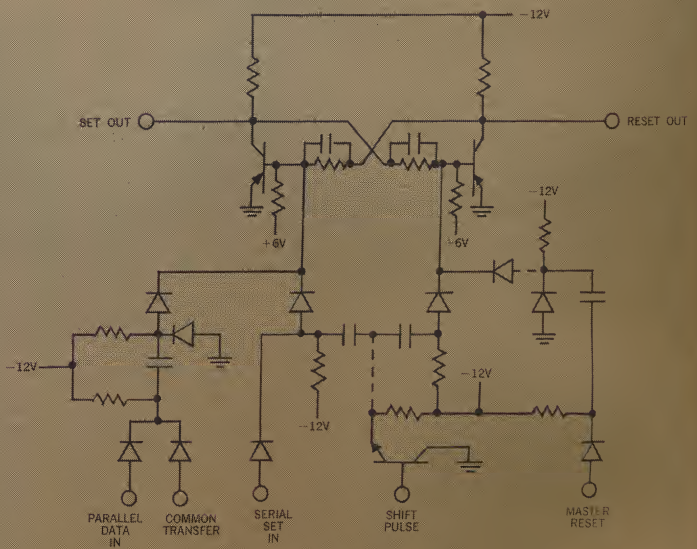
The GSR4 is a four-stage shift register designed to operate in serial-parallel, parallel-serial, or serial-serial modes.

The set side of each flop-flop provides parallel data entry through a two-input AND gate. The other inputs to each AND gate are connected together for a common transfer input. A ONE is entered into the flip-flop when the parallel data input is at binary ONE and the common transfer input goes from binary ONE to binary ZERO. The register should be in the reset state before parallel data is entered. A master reset input is provided to reset all four stages simultaneously.

Serial entry is provided by means of two two-input set and reset AND gates connected to the first flip-flop of the register. One input of each gate is connected together for the shift pulse input. The serial Set and serial Reset data inputs should always be complements of each other. A ONE is entered into the first stage when the set input is at binary ZERO and the shift pulse input goes from binary ONE to binary ZERO.

The outputs may be taken serially from a given flip-flop, in parallel from all flip-flops at once, or in some serial-parallel combination. Additional shift registers may be cascaded to form a register of any length.





SPECIFICATIONS

MODULE	200 KC GSR4-.2	1 MC GSR4-1	5 MC GSR4-5
SHIFT REGISTER			
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (−10V nominal)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (0V nominal)	0 to −1V	0 to −1V	0 to −1V
Shift, Set, Reset & Parallel			
Minimum Amplitude	8V	8V	7V
Maximum Rise Time	1μs	0.25μs	60ns
Minimum Dwell (at binary one level)	2μs	0.4μs	80ns
Input Load			
Common Transfer	4 N loads	4 N loads	8 N loads
Parallel, Serial, Shift	1 N load	1 N load	2 N loads
Noise Rejection	2V	2V	1.5V
Master Reset			
Minimum Amplitude	8V	8V	7V
Maximum Rise Time	1μs	0.25μs	60ns
Minimum Dwell (at binary one level)	10μs	2μs	0.5μs
Input Load	1 N load ½ C2 load	1 N load ½ C1 load	2 N loads ½ C5 load
OUTPUT			
Voltage Levels (full load)			
One (−10V nominal)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (0V nominal)	0 to −0.25V	0 to −0.3V	0 to −0.3V
Maximum Rise Time (no load)	0.25μs	0.1μs	30ns
Maximum Fall Time (no load)	0.5μs	0.2μs	50ns
Maximum Rise Time (full load)	1μs	0.25μs	50ns
Drive Capability	7 N loads 5 P loads 2 C2 loads	7 N loads 10 P loads 2 C1 loads	12 N loads 18 P loads 1 C5 load
Maximum Wiring Capacitance (per output)	1000 pf	300 pf	50 pf
PROPAGATION DELAY	0.2μs	0.1μs	60ns
POWER REQUIREMENTS (per card)			
−12V	107ma	110ma	130ma
+ 6V	1.8ma	1.7ma	2.3ma

GMX1
DIGITAL MULTIPLEXER

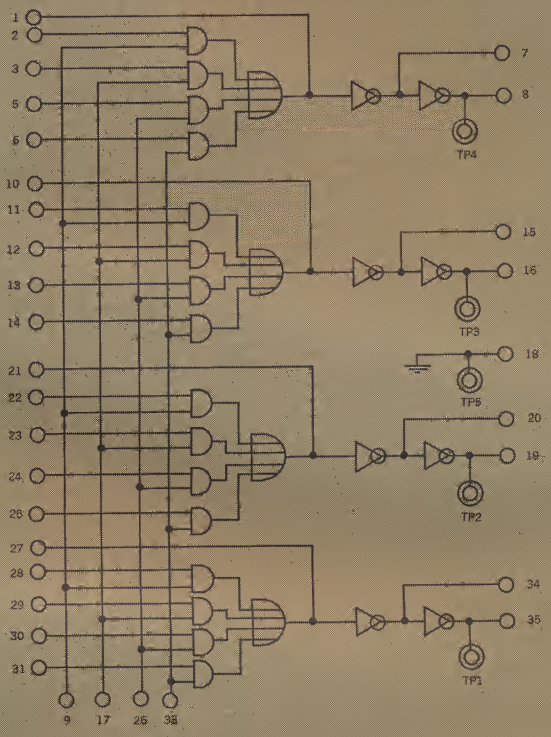
KEY SLOTS PINS 13, 15

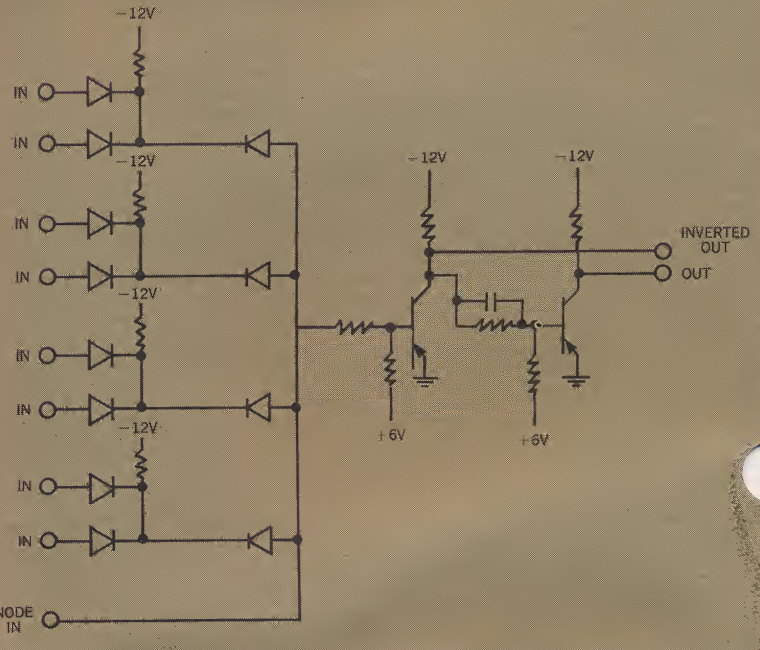
The GMX1 contains four AND/OR gates. Each gate has 8 inputs, a level restoring output, and an inverted output.

For multiplexing purposes, corresponding AND inputs of the four gates are internally connected. These common points are available at pins 9, 17, 26 and 33. This arrangement allows the remaining inputs to be strobed or time shared sequentially.

SPECIFICATIONS

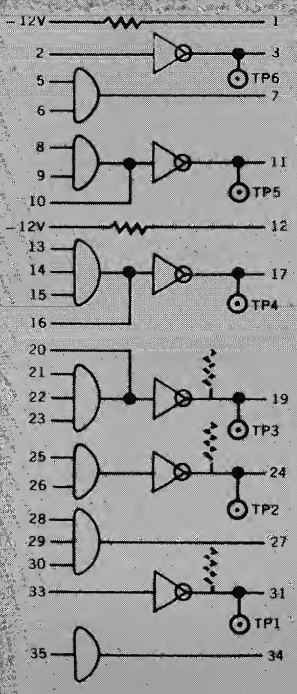
MODULE	200 KC
DIGITAL MULTIPLEXER	
INPUT:	
Frequency	0 to 200 Kc
Voltage Levels	
One (nominal —10V)	—9 to —12V
Zero (nominal —0)	—1 to 1V
Maximum Rise Time	1.0μs
Input Load	2 N loads
OUTPUT:	
Voltage Levels (full load)	
One (nominal —10V)	—9 to —12V
Zero (nominal 0)	0 to —.5V
Maximum Rise Time (no load)	0.1μs
Maximum Fall Time (no load)	9.5μs
Maximum Rise Time (full load)	0.5μs
Drive Capability	
Non-inverted output	8 N loads 7 P loads 4 C2 loads
Inverted output	8 N loads 5 P loads 4 C2 loads
PROPAGATION DELAY	0.2μs
NOISE REJECTION	2.0V
POWER REQUIREMENTS (per card)	
—12V (Pin 32)	150.0 MA
+ 6V (Pin 4)	7.0 MA
Gnd (Pin 18)	

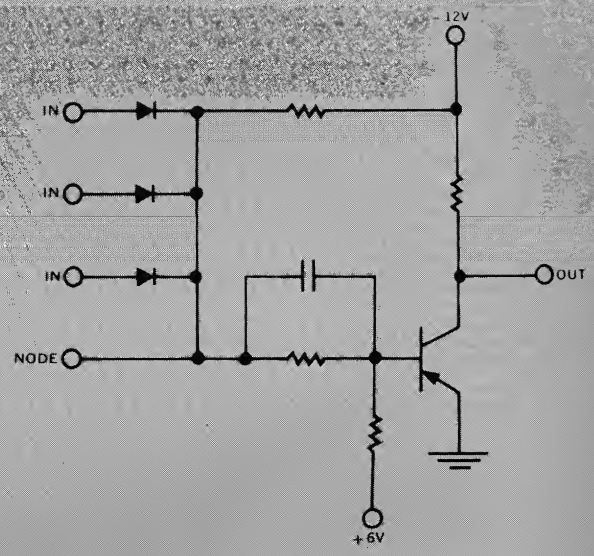




GNA1
NAND GATE

KEY SLOTS PINS 13, 29





The GNA1 has three two-input and three three-input NAND Gates. The NAND Gate has a diode AND Gate followed by an inverter providing the NOT AND function. One two-input and one three-input diode gate are not connected to the inverters. These may be used for expansion of the other gates. For example, a six-input gate may be made by connecting pin 20 to pin 27. Additional gate expansions are made in a similar manner. Extra inverters may then be used for logic inversion.

The NAND Gate provides logic level restoration and more drive capability than diode gates. The AND function may be implemented by following the NAND Gate with an inverter. The OR function may be implemented by using the complements as inputs. For example, with inputs $\overline{A}$ and $\overline{B}$, the output of the NAND Gate is A OR B. Two NAND Gates in series provide AND-OR gating.

Three of the output inverters have the collector load resistor disconnected from the transistor. This allows the connection of two or more NAND Gates in parallel using a single load resistor to form the (AND-OR) NOT function. Inverters with dotted line resistors have internal load resistors.

NOTE: When operating the GNA1 at less than ½ maximum rated frequency, the drive capability for capacitive loads is doubled.

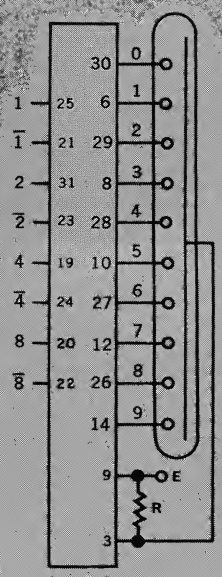
NOTE: Extra resistors on pins 1 and 12 may be used as gate resistors or collector load resistors. Diode clusters do not have internal load resistors.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
NAND GATE	**GNA1-.2**	**GNA1-1**	**GNA1-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (Nominal −10V)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (Nominal 0V)	+1 to −1V	+1 to −1V	+1 to −1V
Maximum rise time	2.5μs	0.5μs	100ns
Maximum fall time	2.5μs	0.5μs	100ns
Input Load	1 N load	1 N load	2 N loads
Noise Rejection	2.0V	1.5V	1.5V
OUTPUT			
Voltage Levels (full load)			
One (Nominal −10V)	−8.6 to −12V	−7.6 to −12V	−8.6 to −12V
Zero (Nominal 0V)	0 to −0.25V	0 to −0.5V	0 to −0.5V
Maximum rise time (no load)	0.25μs	0.1μs	30ns
Maximum fall time (no load)	0.5μs	0.2μs	70ns
Maximum rise time (full load)	1μs	0.25μs	60ns
Drive Capability	10 N loads 5 P loads 2 C2 loads	8 N loads 8 P loads 2 C1 loads	10 N loads 20 P loads 1 C5 load
Maximum wiring capacitance	1000pf	300pf	50pf
PROPAGATION DELAY in chain of NAND gates between consecutive outputs (full load)	0.2μs	0.1μs	40ns
POWER REQUIREMENTS			
per card			
−12V (pin 32)	60ma	80ma	100ma
+6V (pin 4)	2.5ma	2.2ma	2ma
Gnd (pin 18)			

GND1
NIXIE DRIVER

KEY SLOTS PINS 3, 11



The GND1 is comprised of a decoding matrix and 10 amplifier circuits. With an 8-4-2-1 binary coded decimal input the GND1 will drive any Miniature, Standard, or Super Burroughs Nixie indicator. Recommended anode supply voltage (E) and series current limiting resistor (R) for 13 Nixie types are tabulated.

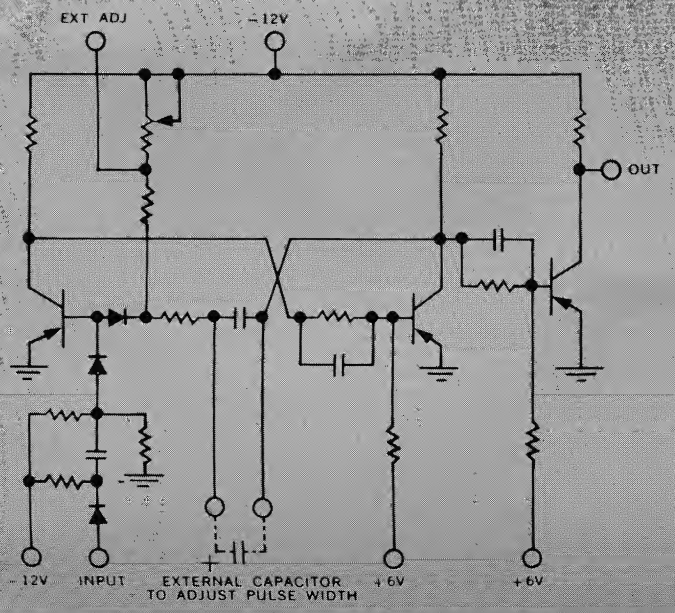
This driver is not suitable for driving the alpha numeric Nixie indicator.

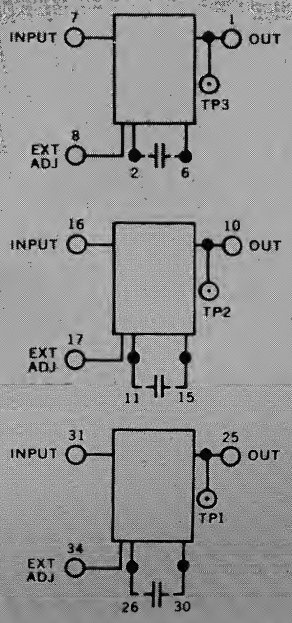
GND1

Recommended Operating Conditions				
Nixie Tube		Anode Supply Voltage	Anode Current	Series Anode Resistor (R)
Miniature	7009	250V	0.95ma	150K ¼W
	7977 (B4032)	250V	1.05ma	91K ¼W
	B4021	150V	1.05ma	33K ¼W
	B4081	250V	1.05ma	150K ¼W
Standard	B5092	250V	2.25ma	56K ½W
	8037 (B5031)	250V	2.25ma	56K ½W
	6844A	250V	2.25ma	56K ½W
Rectangular	B5991	250V	2.25ma	47K ½W
Super	B6091	250V	3.0ma	39K 1.0W
	B6033	250V	3.0ma	39K 1.0W
	7153	250V	2.5ma	43K 1.0W
Large	B8091	250V	4.75ma	22K 1.0W
Jumbo	B7094	300V	5.5ma	27K 2.0W

SPECIFICATIONS

MODULE	
NIXIE DRIVER	**GND1**
INPUT	
Voltage	
One (—10V nominal)	—9 to —12V
Zero (0V nominal)	+1 to —1V
Input Load	6N
OUTPUT	
Burroughs "Nixie" tubes, (See Table)	
POWER REQUIREMENTS per card	
—12Vdc (pin 32)	100ma
+ 6Vdc (pin 4)	6.5ma
Gnd (pin 18)	





GOS3
ONE-SHOT MULTIVIBRATOR

KEY SLOTS PINS 19, 29

The GOS3 has three independent Monostable multivibrator circuits. Each circuit has a potentiometer for pulse width adjustment over a 3 to 1 range. For the narrowest pulse width, the adjustment range is 2 to 1. In the normal (quiescent) state, the output is at binary zero, (OV). The circuit does not respond to the negative going portion of any signal. When the circuit is triggered, the output goes to binary one (−12V). It stays in this state for a length of time determined by the value of an external capacitor (if any) and the setting of the potentiometer. At the end of the preset time, the circuit triggers back to the quiescent state.

The GOS3 may be used for generating pulse widths or pulse delays. The circuit is useful for temporary storage of a single bit or for generating a single pulse from sources which have contact bounce such as relays and switches. Set the one-shot for a pulse width longer than the maximum bounce time.

A connection is available for remote adjustment of the delay by connection of a 10K potentiometer to −12 Volts and the remote adjust pin.

The maximum pulse width (delay) is 70% of the total period.

NOTE: The approximate value of the capacitor needed for any given pulse width may be found by using the formula:

$$C = 100T$$

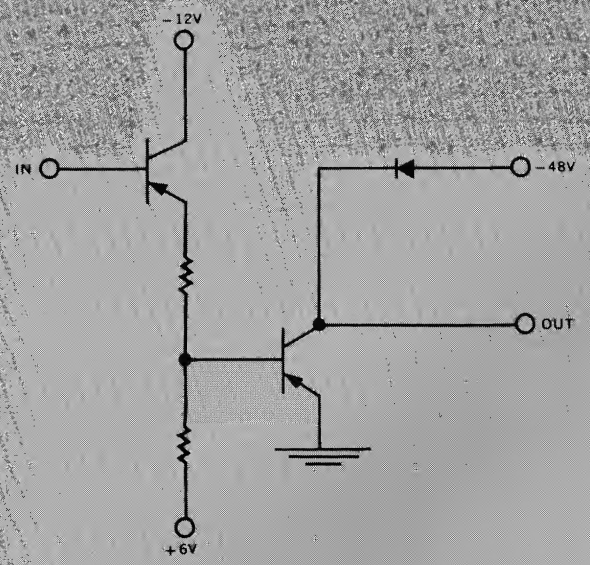
where C is in pf, T is in μs

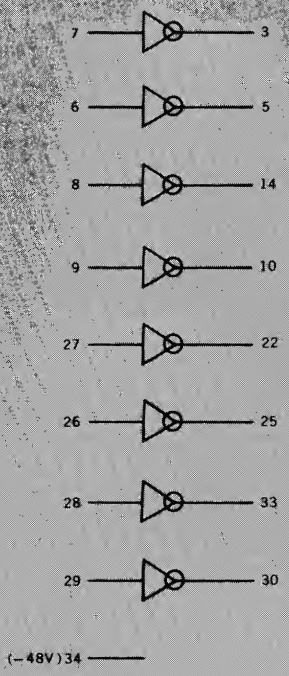
Maximum delay is 1 sec.

NOTE: When operating the GOS3 at less than ½ maximum rated frequency the drive capability for capacitive loads is doubled.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
MULTIVIBRATOR (one shot)	**GOS3-.2**	**GOS3-1**	**GOS3-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (Nominal −10V)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (Nominal 0V)	+1 to −1V	+1 to −1V	+1 to −1V
Set & Reset Inputs			
Minimum Amplitude	8V	8V	7V
Minimum dwell at binary one level	2μs	0.4μs	80ns
Maximum rise time	1μs	0.25μs	60ns
Maximum fall time	2.5μs	0.5μs	100ns
Input load	1 N load	1 N load	2 N loads
Noise Rejection	2V	2V	2V
OUTPUT			
Voltage Levels (full load)			
One (Nominal −10V)	−10 to −12V	−8.5 to −12V	−7.5 to −12V
Zero (Nominal 0V)	0 to −0.25V	0 to −0.5V	0 to −0.5V
Pulse width (no external C)	2.5μ to 5μ	0.5μs to 1.5μs	0.1μs to 0.2μs
Maximum rise time (unloaded) (with no ex. C)	0.25μs	0.1μs	30ns
Maximum fall time (unloaded) (with no ex. C)	0.5μs	0.2μs	70ns
Drive Capability	12 N loads 12 P loads 4 C2 loads	10 N loads 18 P loads 4 C1 loads	20 N loads 25 P loads 2 C5 loads
Maximum wiring capacitance per output	1000pf	300pf	50pf
PROPAGATION DELAY From 10% of the rising trigger to 10% of rising output (full load and minimum pulse output)	0.3μs	0.15μs	40ns
POWER REQUIREMENTS per card			
−12V (pin 32)	105ma	125ma	150ma
+6V (pin 4)	2ma	2ma	2ma
Gnd (pin 18)			





GPA1
POWER AMPLIFIER

KEY SLOTS PINS 17, 27

The GPA1 has 8 independent power amplifier circuits designed for driving relays or incandescent lamps directly from digital logic units. An input emitter-follower is included to minimize the input power requirements.

The GPA1 output is a solid state switch which is closed to ground when the input is at binary "1" and "open" when the input is at binary "0." Leakage current through the load in the "open" condition is typically less than 3 ma.

DRIVING RELAYS

A reverse surge clamping diode is included to prevent the coil inductive surge from damaging the output power transistor.

If the load voltage is not returned to the module, a clamp diode should be connected across the coil with the anode end connected to the relay voltage. The relay voltage common should be connected to the module voltage common. The external clamp diode should be of sufficient size to withstand the maximum current and voltage of the load.

DRIVING LAMPS

When incandescent lamps are first turned on, there is a momentary surge of current which is approximately 10 times the steady state current. Therefore, the maximum load for lamps is less than it is for relays. Clamp diodes are not needed for driving lamps.

SPECIFICATIONS

MODULE	
POWER AMPLIFIER	**GPA1**
INPUT	
Frequency	0 to 2 Kc
Voltage	
One (—10V nominal)	—8 to —12V
Zero (0V nominal)	+1 to —1V
Input Load	2 P loads
OUTPUT	
Voltage	—48V max.
Current	350 ma max.
POWER REQUIREMENTS per card	
—12Vdc (pin 32)	120ma
+ 6Vdc (pin 4)	40ma
Gnd (pin 18)	

GPA2
POWER AMPLIFIER

KEY SLOTS PINS 19, 21

The GPA2 module consists of twelve independent power amplifiers used to drive up to 150 m.a. and/or 28 volts of collector current and voltage, respectively. The output of each amplifier is connected directly to the collector to facilitate driving any load within the specified limits.

These circuits are especially useful in driving relays and indicator lamps.

When using these circuits to drive relays a diode should be shunted across the coil to prevent the coil inductive surge from damaging the transistors. The anode end of the diode should be connected to the relay voltage (1) and it should be sufficient to withstand the maximum current and voltage of the load.

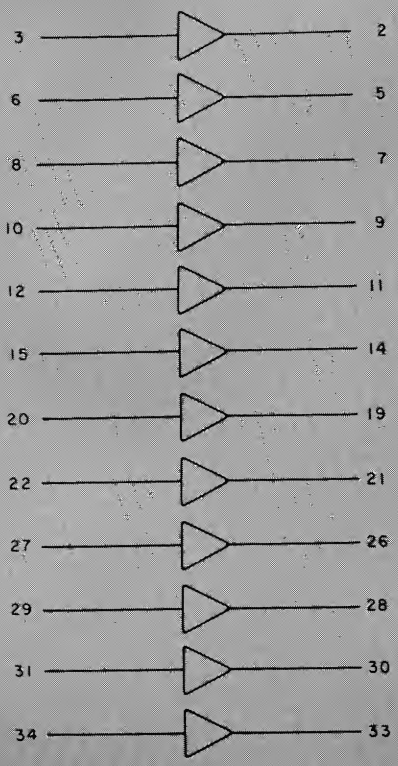
When using these circuits to drive incandescent lamp, a resistor approximately 1/10 RL (resistance of lamp) should be connected in series with the lamp. This will prevent initial surge current from damaging the transistors.

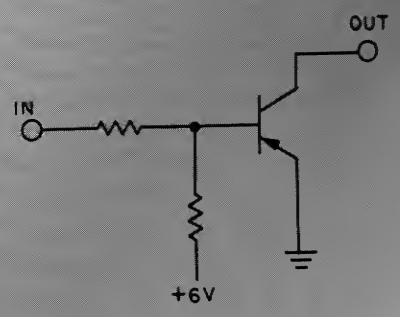
When driving lamps less than 80 ma this resistor is not necessary.

The load must be returned to a negative voltage. When the GPA2 input is at binary 1, the output is 0V.

SPECIFICATIONS

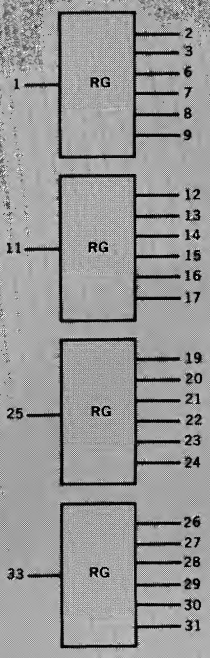
POWER AMPLIFIER	GPA2
INPUT	
Frequency	0 to 5KC
Voltage Levels	
One (nominal —10v)	—9 to —12V
Zero (nominal 0v)	—1 to 1V
Max Rise Time	2.5μs
Max Fall Time	2.5μs
Input Load	5 P load
OUTPUT	
Max Fall Time	10μs
Max Rise Time	5μs
Max Voltage	—28V
Max Current	150ma
Power Requirements (per card):	
+6V (pin 4)	3.8 ma
Gnd (pin 18)	

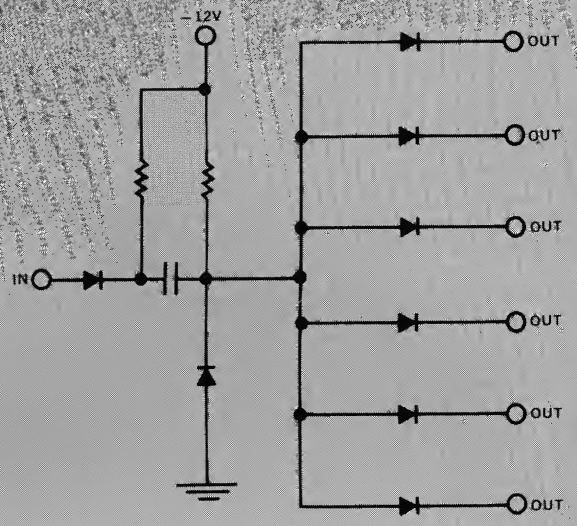




GRG1
RESET GATE

KEY SLOTS PINS 17, 33





The GRG1 has 4 independent reset circuits each capable of resetting 6 flip-flops.

The output of the circuit is connected to the *auxiliary* input of flip-flops to provide MASTER RESET capabilities. When a positive going level shift with the proper amplitude, rise time and pulse width is applied to one of the gate inputs, a pulse is coupled through to reset the flip-flop. The pulse width out of the RESET Gate is of sufficient duration to keep the flip-flop in the reset state while all interconnected flip-flops settle.

NOTE: The auxiliary input to the flip-flop is connected directly to the base of the transistor. Since this is a relatively sensitive point, the reset gate should be located close to the flip-flops being reset.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
RESET GATE	**GRG1-.2**	**GRG1-1**	**GRG1-5**
INPUT			
Maximum repetition rate	40 Kc	200 Kc	1 Mc
Voltage Levels			
One (nominal −10V)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (nominal 0V)	+1 to −1V	+1 to −1V	+1 to −1V
Minimum Amplitude	8V	8V	7V
Maximum rise time	1μs	0.25μs	60ns
Minimum dwell at binary one level	17μs	2.4μs	480ns
Input Load	1 N load ½ C2 load	1 N load ½ C1 load	2 N loads ½ C5 load
Noise Rejection	2.0V	2.0V	1.5V
OUTPUT			
Voltage Levels (full load)			
Input rising to gnd.	+7 to +12V	+6 to +12V	+5 to +12V
Steady state	0 to −1.0V	0 to −1.0V	0 to −1.0V
Maximum rise time	Same as input	Same as input	Same as input
Maximum loading per output Flip-Flop (Aux. input)	1	1	1
Maximum wiring capacitance per output	200pf (very critical)	75pf (very critical)	20pf (very critical)
PROPAGATION DELAY	10ns	10ns	10ns
POWER REQUIREMENTS per card			
−12V (pin 32)	3ma	3ma	3ma
+6V (pin 4)	0	0	0
Gnd (pin 18)			

GRR1
GRR2
REED RELAYS

KEY SLOTS PINS 25, 29 (GRR1)
KEY SLOTS PINS 29, 31 (GRR2)

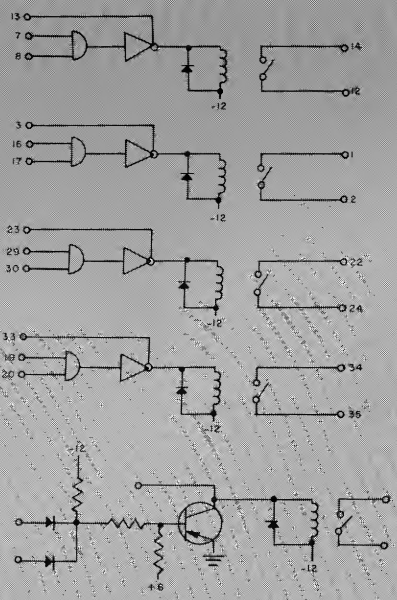
The GRR1 Module contains four (4) dry reed relays and their respective relay driver circuits. The GRR2 contains eight (8) dry reed relays. Each relay contains one (1) form A (normally open) set of contacts. Each of the relay driver circuits is gated by a two input AND gate. One end of each relay coil is available for connection to an external driver circuit.

When the respective relay driver circuit is used, the relay will operate as follows: If both driver inputs are logical ONE (nominal —10V) the relay will be energized, and if either of the driver inputs are logical ZERO (nominal 0V) the relay will be de-energized. If only one input is used the other input may be left open.

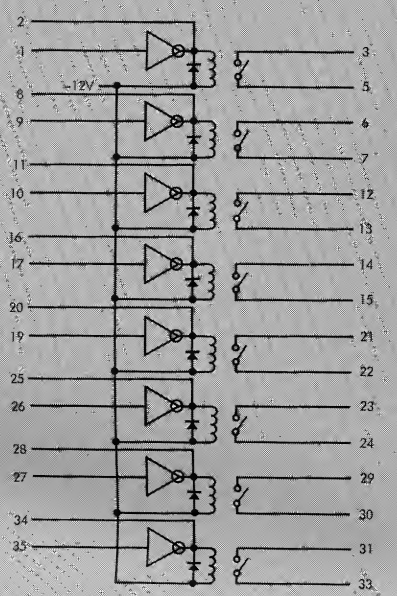
The relay may be operated by an external driver circuit such as the GAI2-.2. The relay requires a nominal 0 volt level to energize and a nominal —12 volt level to de-energize.

When the external driver is used the relay may be energized by either the internal or external driver.

GRR1

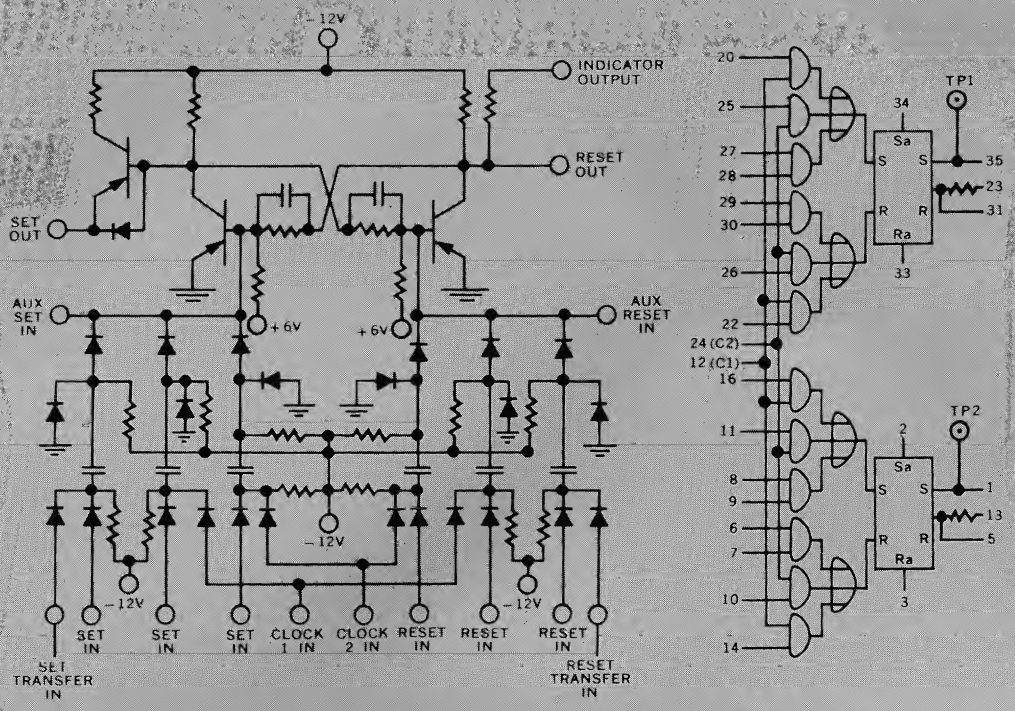


GRR2



SPECIFICATIONS

REED RELAY	GRR1	GRR2
INPUT		
Driver Input		
Frequency	0 to 100 CPS	0 to 100 CPS
Voltage Levels		
One (Nominal —10V)	—8V to —12V	—8V to —12V
Zero (Nominal 0V)	1V to —1V	1V to —1V
Load	2 N Loads	4 P Loads
Noise Rejection		2V
Coil Input Frequency	0 to 100 CPS	0 to 100 CPS
Voltage Levels		
Operate Voltage	1V to —1V	1V to —1V
Release Voltage	—11V to —12V	—10V to —12V
Load	14 N Loads	4 N Loads
Max. Rise Time	5μsec	5μsec
OUTPUT		
Al external inductive loads must have arc suppression circuits for the following contact ratings to be valid.		
Contact Ratings:		
Operate Time (with bounce)	4msec	4msec
Release Time	3msec	3msec
Contact Resistance	100mΩ	200mΩ
Max. Power	15VA	10W
Max. Current (Switching)	1A	0.5A
Max. Voltage (Switching)	200V	200V
Note that the product of the current and voltage shall never exceed 15 VA.		
POWER REQUIREMENTS		
Per Card		
—12V (pin 32)	120ma	82ma
+6V (pin 4)	3.5ma	3ma
Gnd (pin 18)		



GSR2

SHIFT REGISTER

BIDIRECTIONAL

KEY SLOTS PINS 5, 9

The GSR2 contains two flip-flops with extensive input gating. The SET and RESET inputs each have 3 — two input diode AND Gates followed by a three input AC coupled OR Gate. The Set output is buffered for driving long lines. This circuit is extremely versatile and may be used for the following applications:

1. SHIFT REGISTER, serial or parallel input, shift right, shift left, serial or parallel output. Connect pin 35 to 16, 31 to 14, 1 to 25, 5 to 26. Use pin 20 for Serial SET in, pin 22 for Serial RESET in, pin 12 for Shift right, pin 24 for Shift left, pin 1 for SET out and pin 5 for RESET out. Parallel jamb transfer entry may be made by using pins 27 and 8 for parallel SET inputs, pins 30 and 7 for parallel RESET inputs and connecting pins 28, 29, 6 and 9 for the parallel transfer signal input.

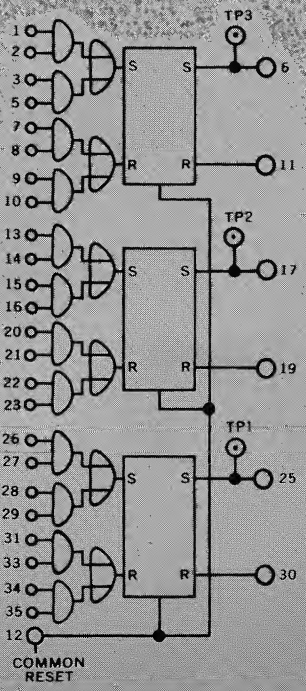
2. Combination BINARY COUNTER — SHIFT RIGHT AND LEFT REGISTER. Use the same pin connections as previously indicated except for the parallel entry. For binary counting, connect pin 35 to 30, 31 to 27, 1 to 7 and 5 to 8 to form the J-K steering. Connect pin 28 to 29, and pin 6 to 9 for use as trigger inputs. Parallel entry may be made through input gate GIG1 into the auxiliary SET or auxiliary RESET inputs.

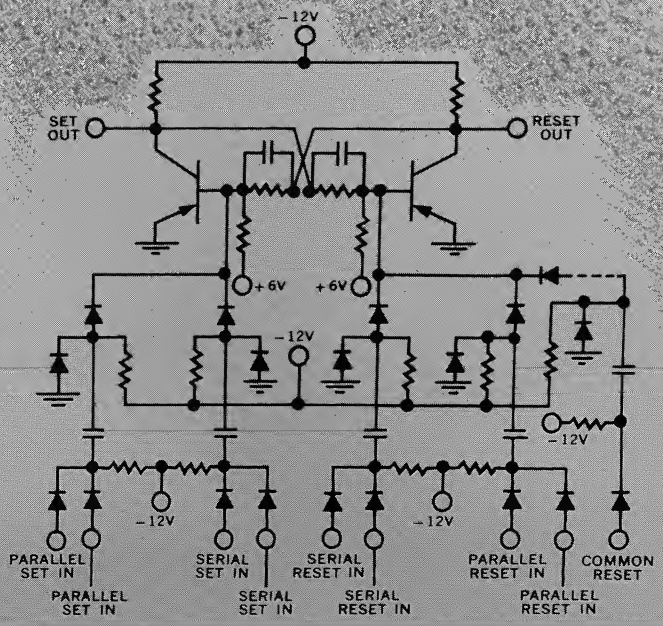
SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
SHIFT REGISTER (bidirectional)	**GSR2-.2**	**GSR2-1**	**GSR2-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (—10V nominal)	—9 to —12V	—8 to —12V	—7 to —1
Zero (0V nominal)	+1 to —1V	+1 to —1V	+1 to —1
Clock input and unclocked inputs			
Min. Amplitude	8V	8V	7V
Max. rise time	1μs	0.25μs	60 ns
Min. dwell at binary one level	2μs	0.4μs	80ns
Clock input load	4 N loads	4 N loads	8 N loads
Set, reset input load	1 N load	1 N load	2 N loads
Noise Rejection	2V	2V	1.5V
Minimum positive noise input for output disturbance of less than 0.5V			
OUTPUT			
Voltage Levels (full load)			
One (—10V nominal)	—9 to —12V	—8 to —12V	—7 to —12
Zero (0V nominal)	0 to —0.25V	0 to —0.3V	0 to —0.3
Maximum rise time (no load)	0.25μs	0.1μs	30ns
Maximum fall time (no load)	0.5μs	0.2μs	50ns
Maximum rise time (full load)	1μs	0.25μs	50ns
Drive Capability			
Set Output	10 N loads 55 P loads 6 C2 loads	9 N loads 80 P loads 6 C1 loads	14 N loads 100 P loads 6 C5 loads
Reset Output	10 N loads 5 P loads 2 C2 loads	9 N loads 10 P loads 2 C1 loads	14 N loads 18 P loads 1 C5 loads
Maximum wiring capacitance per output	1000pf	300pf	50pf
PROPAGATION DELAY From 10% of rising clock pulse to 10% of rising output (full load)	0.2μs	0.1μs	60ns
POWER REQUIREMENTS per card			
—12V (pin 32)	65ma	75ma	95ma
+6V (pin 4)	1.0ma	1.5ma	1.0ma
Gnd (pin 18)			

GSR3
SHIFT REGISTER

KEY SLOTS PINS 19, 27





The GSR3 has three gated flip-flops for serial and parallel input and output or for shift right and shift left operation. Several GSR3 modules may be cascaded to form a register of any length. Parallel input is effected by means of two 2-input diode AND gates. One input to each gate is the parallel set and reset input. The parallel SET and RESET inputs should always be complements of each other. The other input to each gate is used for the transfer pulse. With this circuit the jamb transfer may be used to enter information in the register without the necessity of first clearing the register.

Serial input is effected by means of two 2-input diode AND gates. The serial SET and RESET inputs should always be complements of each other. The shift signal should be a standard clock signal.

When using the parallel in, serial out mode the SERIAL SET input may be connected to OV so that after the information is shifted out, the register will end up in the reset condition.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
SHIFT REGISTER (bidirectional)	**GSR3-.2**	**GSR3-1**	**GSR3-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Voltage Levels			
One (−10V nominal)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (0V nominal)	+1 to −1V	+1 to −1V	+1 to −1V
Clock input & unclocked inputs			
Minimum amplitude	8V	8V	7V
Maximum rise time	1μs	0.25μs	60ns
Minimum dwell at binary one level	2μs	0.4μs	80ns
Input Load	1 N load	1 N load	2 N loads
Common Reset Input			
Minimum amplitude	8V	8V	7V
Maximum rise time	1μs	.25μs	60ns
Minimum dwell at binary one level	10μs	2μs	0.5μs
Input load	1 N load ½ C2 load	1 N load ½ C1 load	2 N loads ½ C5 load
Noise Rejection Minimum positive noise input for output disturbance of less than 0.5V	2V	2V	1.5V
OUTPUT			
Voltage Levels (full load)			
One (−10V nominal)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (0V nominal)	0 to −0.25V	0 to −0.3V	0 to −0.3V
Maximum rise time (no load)	0.25μs	0.1μs	30ns
Maximum fall time (no load)	0.5μs	0.2μs	50ns
Maximum rise time (full load)	1μs	0.25μs	50ns
Drive Capability	10 N loads 5 P loads 2 C2 loads	9 N loads 10 P loads 2 C1 loads	14 N loads 18 P loads 1 C5 load
Maximum wiring capacitance per output	1000pf	300pf	50pf
PROPAGATION DELAY From 10% of rising clock pulse to 10% of rising output (full load)	0.2μs	0.1μs	60ns
POWER REQUIREMENTS per card			
−12V (pin 32)	55ma	65ma	85ma
+6V (pin 4)	1.4ma	1.5ma	1.5ma
Gnd (pin 18)			

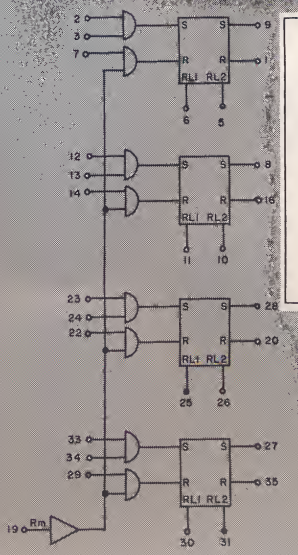
GSS1
SILICON SWITCH

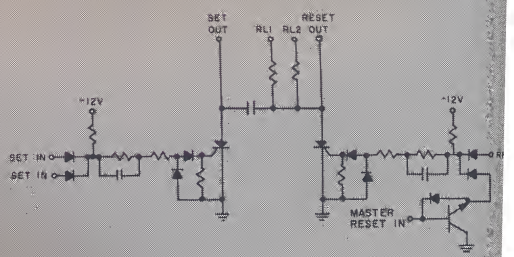
The GSS1 has four (4) identical Silicon Switch Circuits. Each of these circuits can function as either a power flip-flop or a high gain—high power switch. With this circuit, relatively high currents and voltages that cannot be switched by the normal transistor logic circuits can be switched.

Each circuit has two SET INPUTS and one RESET INPUT with an additional MASTER RESET input that furnishes a reset trigger to all four circuits simultaneously. When the proper positive going input signal is present at any one of these inputs, its respective OUTPUT will turn on and switch to ground.

When a trigger (positive going edge of a negative pulse) is applied to a SET INPUT the SET OUTPUT will turn on and switch to ground. This will cause the RESET OUTPUT to turn off and stop the current flow through its load. If it is desired to again turn on the RESET OUTPUT (or turn off the SET OUTPUT) a reset trigger is applied either to the RESET INPUT or the MASTER RESET and the RESET OUTPUT is turned on and the SET OUTPUT is turned off. To operate as a power flip-flop both the SET OUTPUT and the RESET OUTPUT will be loaded externally; when it is desired to switch only one output, the SET OUTPUT is loaded externally and the RESET OUTPUT is loaded either internally or externally. (See Note 2).

If simultaneous SET and RESET trigger pulses are applied or if the maximum frequency is exceeded, both outputs will turn on. To return to normal operation, remove the anode voltage momentarily.





SPECIFICATIONS

SILICON SWITCH	GSS1
INPUT	
Frequency	See Notes 1 & 2
Voltage Levels	
One (—10V nominal)	—8.5 to —12V
Zero (0V nominal)	1 to —0.5V
Set or Reset Trigger	
Min. Amplitude	8V
Min. dwell at binary one level	70μsec
Max. rise time	1.0μsec
Input Load	5N
Master Reset Trigger	
Min. Amplitude	8V
Min. dwell at binary one level	70μsec
Max. rise time	1.0μsec
Input load	1N
Minimum Pulse Width (At Binary Zero Level)	4μsec
Noise Rejection	2V
OUTPUT	
Drive Capability (SET & RESET)	
Voltage Range	25 to 100 VDC
Current Range (Over entire voltage range)	10 to 200ma
Max. Surge Current 100 μsec max. surge current duration 10% maximum duty cycle	1.0 Amp
Max. Fall Time (Negative going)	4μsec
Max. Rise Time (Positive going)	See Note #3
Max. Capacitive Load	0.01μf
POWER REQUIREMENTS	
—12V	10ma

NOTES:

1. The maximum operating frequency of the GSS1 depends on the value of load resistance in the SET and the RESET anode circuits. The SET OUTPUT will always be loaded externally, however, the RESET OUTPUT may be loaded either externally or internally. The maximum allowed frequency of operation may be found by solving the formula below.

$$f\,Max = \frac{10^6}{4\,RL\ (Max)}\ C.P.S.$$

Where:

The units of RL (Max) are ohms.
RL (Max) is the larger of the anode load resis
For Example: If the SET OUTPUT anode load
ance is 600Ω and the RESET OUTPUT anod
resistance is 1,000Ω, then RL (Max) = 1,000Ω
Max = 250 CPS.

If the RESET OUTPUT is internally loaded th
of anode resistance may be obtained from Tab
Note 2. (See RLR).

The absolute maximum frequency for the device
This is obtained when both outputs are loaded wi
and returned to 25v.

2. The table below describes the necessary connections
made when the RESET OUTPUT is loaded interna

TABLE 1.

Anode Supply Voltage, VDC	RL1	RL2	RLR Oh
25 to 50	E_{bb}	E_{bb}	5 • 1
51 to 100	E_{bb}	Open	9.75 • 1

Where: E_{bb} is the anode supply voltage.

3. The rise time of the GSS1 circuit depends on the
load resistance in the SET and RESET anode circu
max. rise time may be found from the following for

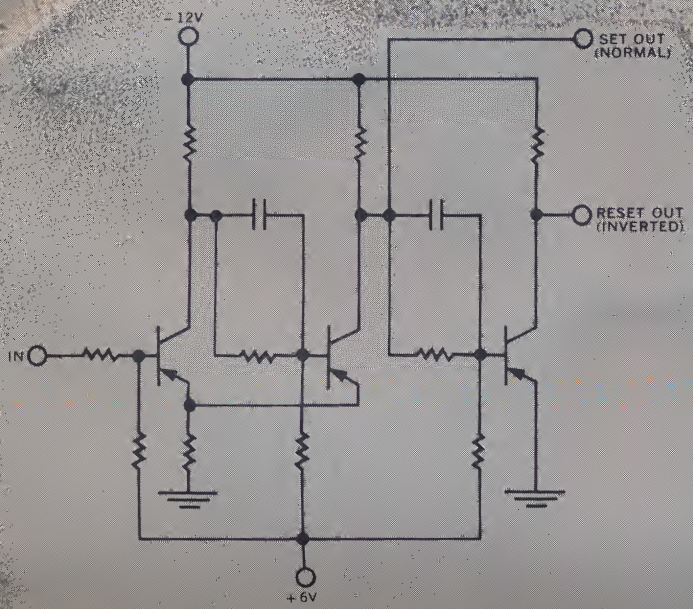
$$t_r\ (Max) = RL\ (Max) \cdot 10^{-6}\ Sec$$

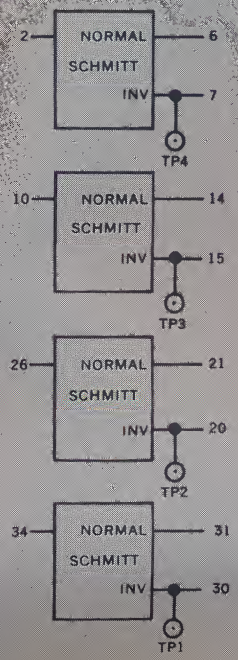
Where:

RL (Max) is the same value as that used to
f Max.
(See Note 1).
Example: If RL (Max) = 1,000Ω then t_r = 1 mse

4. There is a period of time during the switching of th
circuit when the load will be subject to an increase
age across it. This increase in voltage occurs w
OUTPUT in question is being turned off and will
in magnitude to E_{bb} and be present for a maximum
$0.7t_r$.

5. Inductive loads should have a discharge circuit acro
so that the maximum allowable anode voltage will
exceeded.





GST1
SCHMITT TRIGGER

KEY SLOTS PINS 17, 31

The GST1 has four identical and independent Schmitt trigger circuits. It may be used for (1) reshaping of degenerated waveforms, (2) squaring of sinusoidal or non-rectangular waveforms, (3) DC level sensing, (4) inverter, (5) pulse amplifier. Both normal (Set) and inverted (Reset) outputs are available. The nominal threshold level of —4.0V will vary somewhat (±.5V) from unit to unit but is relatively stable for any given unit.

When the input signal goes more positive than the threshold by approximately 0.5V or more, the set output triggers to binary 0 (0V). When the input signal goes more negative than the threshold by approximately 1.0V or more, the set output triggers to binary one (−12V).

To eliminate some of the problems of the more common two transistor Schmitt trigger, the GST1 has three transistors for each circuit. Each output goes through at least two stages of inversion. This provides faster output rise times, more isolation between the input and the output and allows heavier output loading.

NOTE: When using the inverted output of the GST1 at less than ½ maximum rated frequency, the drive capability for capacitive loads is doubled.

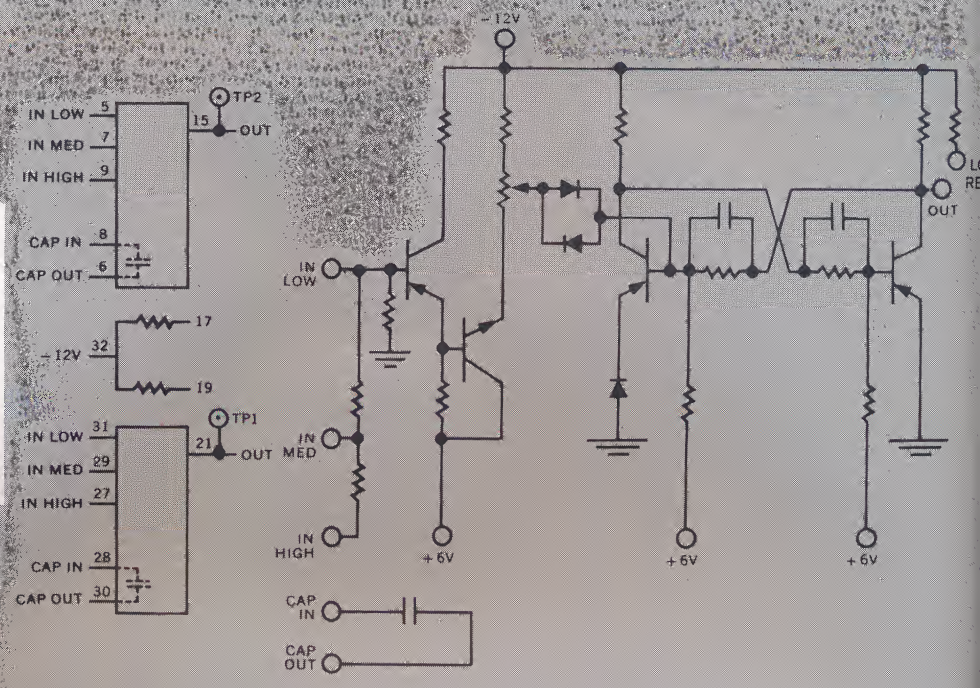
SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
SCHMITT TRIGGER	**GST1-.2**	**GST1-1**	**GST1-5**
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Maximum input	±20V	±20V	±20V
Input Load See NOTE 1	9 P loads (4.7K to gnd.)	11 P loads (3.6K to gnd.)	19 P loads (2.2K to gnd.)
Threshold Level	−3.5 to −4.5V	−3.5 to −4.5V	−3.5 to −4.5V
OUTPUT (Reset side)			
Voltage Levels One (Nominal −10V)	−9.5 to −12V	−8.5 to −12V	−7.5 to −12V
Zero (Nominal 0V)	0 to −0.25V	0 to −0.75V	0 to −0.75V
Typical hysteresis of trigger level	1.5V	1.5V	1.5V
Maximum rise time (no load)	0.25μs	0.1μs	30ns
Maximum fall time (no load)	0.5μs	0.2μs	50ns
Maximum rise time (full load)	1μs	0.25μs	60ns
Drive Capability	10 N loads 7 P loads 4 C2 loads	8 N loads 10 P loads 3 C1 loads	14 N loads 10 P loads 2 C5 loads
Maximum wiring capacitance	1000pf	300pf	50pf
PROPAGATION DELAY From DC triggering level to 10% of output (full load)	0.5μs	0.2μs	50ns
POWER REQUIREMENTS per card			
−12V (pin 32)	60ma	65ma	70ma
+6V (pin 4)	4.5ma	5ma	5ma
Gnd (pin 18)			

NOTE 1: Because the GST1 Schmitt trigger can be triggered by a small signal shift, normal loading rules do not apply. The GST1 may be driven by any of the standard circuits, however, if the drive capability of the drive circuit is exceeded, no other loads should be driven in addition to the GST1.

GST2
SCHMITT TRIGGER
ADJUSTABLE

KEY SLOTS PINS 13, 33



The GST2 has two independent Schmitt trigger circuits. These circuits operate in essentially the same manner as the GST1 Schmitt trigger except that the GST2 has adjustable threshold levels. The GST2 Schmitt triggers also have three separate inputs for low, medium and high signals.

The threshold level of the GST2 circuits may be separately adjusted by means of potentiometers mounted on the card. For low input signals between +6V and —6V, the threshold (trigger) level may be set anywhere between +3.5V and —3.5V.

For example, if the input signal is OV to +6V use the low input. The threshold level may be set at +3V. When the input voltage is more positive than +3V, the output will trigger to binary zero. When the input voltage goes more negative than +3V, the output triggers to binary one. The difference between the turn ON voltage and the turn OFF voltage (hysteresis) is typically about 1V.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
SCHMITT TRIGGER	GST2-.2	GST2-1	GST2-5
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5 Mc
Maximum input			
Low input	±6V	±6V	±6V
Medium input	±9V	±9V	±9V
High Input	±12V	±12V	±12V
Typical input load (See Note 1)			
Low input	7 P loads (6K to gnd)	7 P loads (6K to gnd)	14 P loads (3K to gnd)
Medium input	5 P loads (9K to gnd)	5 P loads (9K to gnd)	9 P loads (4.5K to gnd)
High input	4 P loads (12K to gnd)	4 P loads (12K to gnd)	7 P loads (6K to gnd)
Max. Trigger Range Adjustment			
Low input	±3.5V	±3.5V	±3.5V
Medium input	±5V	±5V	±5V
High input	±7V	±7V	±7V
OUTPUT			
Voltage Levels			
One (Nominal —10V)	—9.5 to —12V	—8.5 to —12V	—7.5 to —12V
Zero (Nominal 0V)	0 to —0.25V	0 to —0.5V	0 to —0.5V
Typical Hysteresis of trigger level at DC			
Low input	1.2V	1.2V	1.1V
Medium input	1.8V	1.8V	1.7V
High input	2.5V	2.5V	2.3V
Maximum rise time (no load)	0.25μs	0.1μs	20ns
Maximum fall time (no load)	0.5μs	0.2μs	50ns
Maximum rise time (full load)	1μs	0.25μs	25ns
Drive Capability	18 N loads 7 P loads 4 C2 loads	8 N loads 10 P loads 4 C1 loads	12 N loads 10 P loads 3 C5 loads
With load resistor connected	12 N 21 P 4 C2	2 N 28 P 4 C1	6 N 32 P 3 C5
Maximum wiring capacitance per output	1000pf	300pf	50pf
PROPAGATION DELAY DC Triggering Level to 10% of output (full load)	0.5μs	0.2μs	50ns
POWER REQUIREMENTS per card			
—12V (pin 32)	35ma	40ma	45ma
+6V (pin 4)	8ma	10ma	12ma
Gnd (pin 18)			

NOTE 1. Because the GST2 Schmitt trigger can be triggered by a small signal shift, normal loading rules do not apply. The GST2 may be driven by any of the standard circuits, however, if the drive capability of the drive circuit is exceeded, no other loads should be driven in addition to the GST2.

SPECIFICATIONS

MODULE	200 KC	1 MC	5 MC
DC AND GATE	GUL1-2	GUL1-1	GUL1-5
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	0 to 5Mc
Voltage Levels			
One (−10V nominal)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (0V nominal)	+1 to −1V	+1 to −1V	+1 to −1V
Maximum rise time	1μsec	0.25μsec	60ns
Input Load (nominal)	1 N load*	1 N load*	2 N loads*
OUTPUT			
Voltage Levels (full load)			
One (−10V nominal)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (0V nominal)	+.5V to −1V	+.5 to −1V	+.5 to −1V
Rise time (full load)	Same as input	Same as input	Same as input
Fall time (no load)	Same as input	Same as input	Same as input
Typical Level Shift (output from input)	−0.5V	−0.5V	−0.5V
Drive Capability	10 N* 2 P 1 C2	10 N* 3 P 1 C1	10 N* 8 P 1 C5
Driving Inverters	The AND gate is suitable for driving one Inverter such as the GA12, GD11 or GD12. Because the output voltage level of an AND gate driving an Inverter is shifted out of tolerance for other circuits no loads should be driven in addition to the inverter.		
Maximum wiring capacitance	1000pf	300pf	50pf
PROPAGATION DELAY	10ns	10ns	10ns
INVERTER			
INPUT			
Frequency	0 to 200 Kc	0 to 1 Mc	
Voltage Levels			
One (−10V nominal)	−9 to −12V	−8 to −12V	−7 to −12V
Zero (0V nominal)	+1 to −1V	+1 to −1V	+1 to −1V
Max. Rise Time	2.5μs	0.4μs	100 ns
Max. Fall Time	2.5μs	0.4μs	100 ns
Input Load	5 P loads 1 C2 load	4 P loads 1/2 C1 load	8 P loads 1/2 C5 load
Noise Rejection	1.5V	1.5V	1.5V
Min. Noise input for output disturbance less than 2.0V			
OUTPUT			
Voltage Levels (full load)			
One	−9 to −12V	−8 to −12V	−7 to −12V
Zero	+.5 to −.3V	+.5 to −.3V	+.5 to −.5V
Max. Rise Time (No load)	0.3μs	0.1μs	30 ns
Max. Fall Time (No load)	0.5μs	0.2μs	50 ns
Max. Rise Time (Full load)	1.0μs	0.25μs	60 ns
Drive Capability	5 N loads 5 P loads 4 C2 loads	5 N loads 5 P loads 2 C1 loads	8 N loads 10 P loads 2 C5 loads
Max. Wiring Capacity	1000pf	300pf	50 pf
PROPAGATION DELAY	0.2μs	0.1μs	40 ns
POWER REQUIREMENTS			
per card			
−12V (pin 32)	48ma	48ma	107ma
+6V (pin 4)	0.7ma	0.7ma	1.5ma
Gnd (pin 18)			

*All N type loads driven by the AND gate must be added to the input load of the driver AND gate. For example, if an AND gate is driving 5 other AND gates, each with an input load of 1 N type load, then the effective input load of the first gate is 6 N (1 + 5).

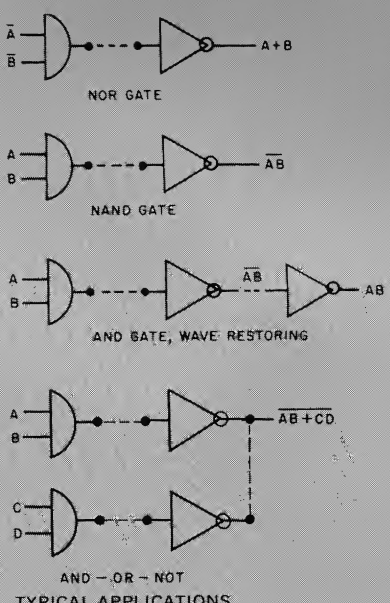
GUL1
UNIVERSAL LOGIC

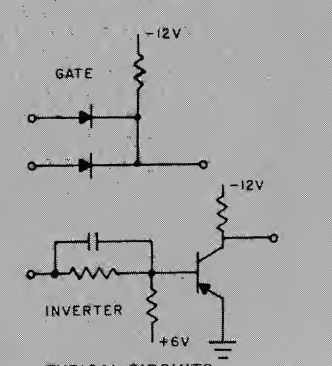
KEY SLOTS PINS 25, 33

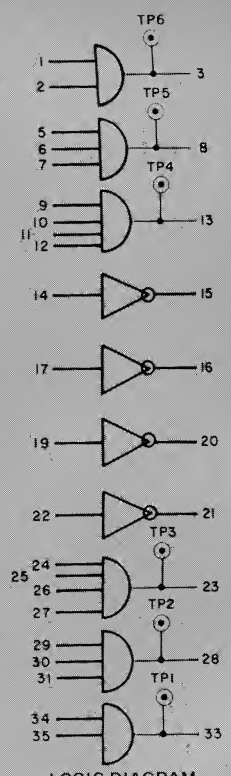
The GUL1 Universal Logic has four (4) inverters and six (6) DC AND gates (2 each of 2-input, 3-input and 4-input gates). Maximum versatility is obtained by use of these circuits in various combinations. They may be used as multiple input AND/OR gates, inverters or non-inverting amplifiers.

AND/OR logic may be obtained by connecting one of the gate inputs to the input of a cascaded inverter. This cascaded inverter also restores logic levels and waveforms, thereby permitting these gates to be cascaded indefinitely.

Two inverters may be cascaded to form a non-inverting amplifier.







20 MC CIRCUITS – – A GENERAL DISCUSSION

The 20 MC digital circuit module line consists of four circuits: The GAI3-20 Inverter; the GFF4-20 Flip-Flop; the GDG4-20 AND Gate; and the GDG5-20 OR Gate. These circuits are suitable for operation from DC to frequencies up to 20 MC.

Power supply voltages required are standard –12 volts and +6 volts with a maximum variation of ±5%. Signal levels are: –6 volts (nominal) equals binary 1; 0 volts (nominal) equals binary 0. The modules are mounted on standard 4¼" x 3¾" x 1/16" epoxy glass cards with 35-pin Varicon connectors.

Logic signal levels used, –6 volts (true) and 0 volts (false), are compatible with Raytheon's existing standard G-series modules described in this catalog. The standard 200 KC, 1 MC and 5 MC line signal levels are 0 volts and –9 volts, 0 volts and –8 volts, and 0 volts and –7 volts, respectively. As frequency is increased, signal levels are decreased accordingly. In order to obtain higher frequencies, switching times (rise and fall times) and circuit delay must decrease so that circuits will operate at maximum frequency.

One way to speed up switching times is to increase current through the circuits so that time constants are decreased. Also, the less the signal is required to swing, the faster the switching times.

Diode signal clamping is not used because of the additional clamping voltage required and because of the danger of accidental shorting when power is on. At 20 MC the clamp diode has a capacitive loading effect which reduces circuit capability. Normal logic requires fewer components and therefore increases reliability.

DESIGN CRITERIA

At 20 MC switching rates, switching from one level into another must be done within about 12 nanoseconds. In addition, wiring and circuit delay must be considered.

For example, a foot of wire may have the following general effects: 1) 1.5 nsec delay; 2) 1 volt of noise for a 15 ma current change due to inductance; and 3) 5 pf capacitance for point-to-point wiring. Wires in a bundle have typically 40 pf capacitance per foot.

All these factors should be considered in system hook-ups due to the critical circuit parameters involved.

SYSTEM DELAY A 10-foot length of wire will cause a delay of 15 nsec which is excessive for operation at 20 MC. Therefore, wire length must be limited to about 5 feet as far as delay is concerned.

INDUCTANCE Maximum signal wire length should be less than 10 ma feet; that is, the wire length in feet times the current change in the wire should not exce 10 ma feet. Input wire leads should be kept to withi 1 or 2 feet.

CAPACITANCE There is approximately 5 pf c capacitance in a foot of wire, depending on the pro imity of its position with respect to the circuit. Capac itance is directly related to frequency and switchin times. Therefore, it is important to keep wire lengt as short as possible. Five feet of wire has approxi mately 25 pf which approaches the maximum circui capacitive load.

GROUND LEADS Ground leads should be as shor as possible and routed throughout the system so tha they are accessible as reference points wherever crit ical measurements are made.

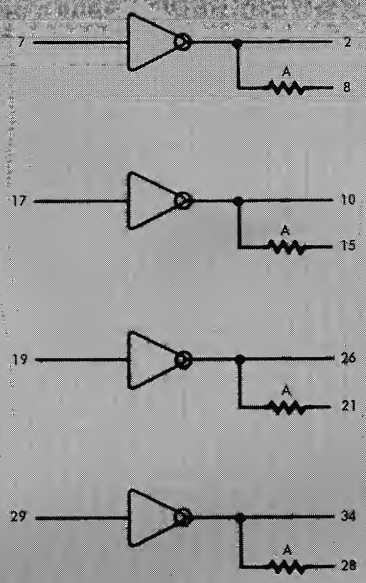
ABOUT THE CIRCUITS

The AND Gate and OR Gate are DCTL (Direc Coupled Transistor Logic) circuits in the Emitte Follower configuration. This type of circuit has th advantage of very fast response times compared t other forms of logic circuits. The output drive capa bility is very good. A maximum of 5N loads and/o 20 P loads may be driven by these circuits. Capaci tance up to 40 pf may be imposed at the outputs.

The Inverter circuit uses DTL (Diode Transisto Logic) circuits consisting of two stages. The firs stage utilizes the non-saturating technique to elimi nate the storage problem of the transistors, thereb decreasing the turn-on and turn-off times of the ci cuit. Three cascaded diodes at the input provide d noise rejection.

The second stage of the Inverter consists of a com plementary emitter-follower circuit to provide goo output drive capability with fast response times. Thi circuit also functions as a signal level restorer. Tw of these circuits may be cascaded to operate as non inverting amplifiers. One inverter plus any combin tion of two AND/OR Gates in series is allowe between flip-flops when operating at 20 MC. Any com bination of three gates may be connected in serie between flip-flops regardless of frequency.

The flip-flop circuit consists of a gated inverter whic couples the input clock signal into the flip-flop. Bo the basic flip-flop and the inverter use the non-sa urated transistor technique for faster switching. Bo a square wave and a sine wave input are provided f maximum versatility. The square wave input is u in most general applications because of the wide f quency range that it may cover (from d.c. to 20 MC) The sine wave input will accept signals from a sin wave generator. However, the frequency range from 5 MC to 20 MC because of the deterioration switching times at lower frequencies.



GAI3-20
AMPLIFIER INVERTER

KEY SLOTS PINS 11, 21

The GAI3-20 consists of four identical amplifier inverter circuits capable of operation at frequencies up to 20 MC. This circuit is used as a logic inverter and as a level and signal restorer for degraded input signals. When the input signal is at binary "1", the output is binary "0". When the input is binary "0" the output is binary "1".

The GAI3-20 is also useful as a heavy duty gate driver or flip-flop driver. Two inverters cascaded (one driving another) will perform the function of non-inverting amplifier and driver. When operating at 20 MC, no more than one inverter should be connected in series between flip-flops.

The GAI3-20 output is buffered by complementary emitter-followers providing extremely fast rise and fall times and the capability of driving loads returned to either a positive or negative voltage.

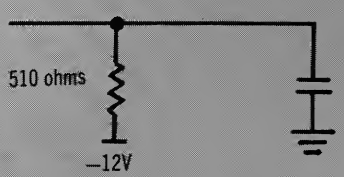
An additional load resistor is internally connected to the output of each inverter circuit. This resistor may be connected to —12 V to provide a different drive combination.

When operating at frequencies below 10 MC, the drive capability as specified for capacitive loads may be doubled.

As in all high frequency circuits, extreme care should be exercised in routing signal wires and in the grounding scheme. Signal and ground connections should be as short as possible. Ground leads should have low impedance.

SPECIFICATIONS

MODULE	20 MC
AMPLIFIER INVERTER	**GAI3-20**
INPUT:	
Frequency	0 to 20 MC
Voltage Levels	
One (—6V nominal)	—4 to —12V
Zero (0V nominal)	+1 to —1V
Maximum Rise Time (to produce specified output)	20nsec.
Input Load (nominal)	2N loads
Noise Rejection	1.5V
OUTPUT:	
Voltage Levels	
One (—6.5V nominal unloaded)	—5.5 to —7.5V (depending on load)
Zero (0V nominal)	0 to —1.0V
Rise Time (typical) (loaded per Fig. 1)	8nsec.
Fall Time (typical) (loaded per Fig. 1)	8nsec.
Drive Capability	10N loads 10P loads 40 pf capacitance
with Resistor A connected to —12V	6N loads 16P loads 60 pf capacitance
PROPAGATION DELAY:	
Measured at —2V level and loaded per Fig. 1	12nsec.

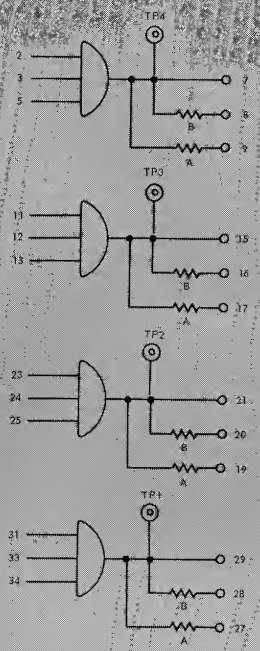


— Figure 1 —

POWER REQUIREMENTS:	
—12V ±5%	30ma (max.)
+6V ±5%	4ma (max.)

GDG4-20
AND GATE

KEY SLOTS PINS 27, 31



The GDG4-20 consists of four identical three-input DC AND Gates capable of operation at frequencies up to 20 MC. The output is binary "1" only when all inputs are binary "1".

DCTL (Direct Coupled Transistor Logic) is used to provide fast response times and good output drive capability. Unused inputs may be left unconnected and do not affect the operation of the units.

AND Gates may be expanded simply by paralleling the outputs of two or three gates. An AND Gate with up to 9 inputs may be implemented in this fashion. When expanded gates are formed in this fashion, the drive capability of the output is 2N loads, 30 P loads, 60 pf capacitance.

Due to the voltage drop across the transistors, the signal amplitude is reduced as it passes through the gate. Most of this reduction occurs as the binary "1" level is shifted in the positive direction.

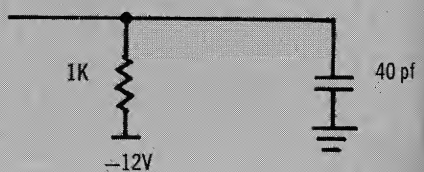
Two resistors are internally connected to the outputs of each gate. One or both of these may be externally connected to —12 V to provide various drive combinations.

When operating at frequencies below 10 MC, the drive capability as specified for capacitive loads may be doubled.

As in all high frequency circuits, extreme care should be exercised in routing signal wires and in the grounding scheme. Signal and ground connections should be as short as possible. Ground leads should have low impedance.

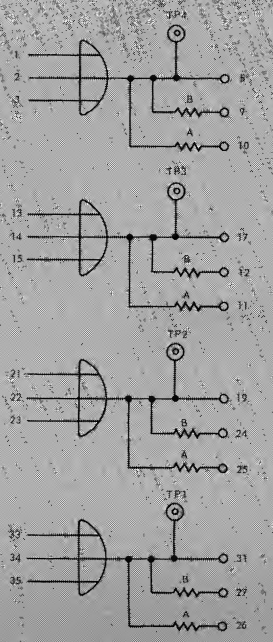
SPECIFICATIONS

MODULE	20 MC
AND GATE	**GDG4-20**
INPUT:	
Frequency	0 to 20 MC
Voltage Levels	
One (—6V nominal)	—4.6 to —7.5V
Zero (0V nominal)	+1 to —1.0V
Rise Time (to produce specified output)	8nsec.
Input load (nominal)	1N Load
OUTPUT:	
Voltage Levels	
One (—6V nominal)	80% of Input Level
Zero (0V nominal)	0 to —0.7V
Rise Time (typical loaded per Fig. 1)	8nsec. (output rise time will equal input rise time when input rise time is more than 8nsec.)
Fall Time (typical)	8nsec.
Typical Level Shift (output from input)	Binary One = +0.9V Binary Zero = +0.1V
Drive Capability	5N loads 20P loads 40 pf capacitance
with Resistor A connected to —12V	1.5N loads 30P loads 60 pf capacitance
with Resistor B connected to —12V	3N loads 25P loads 50 pf capacitance
with Resistors A & B both connected to —12V	0 N loads 35P loads 70 pf capacitance
PROPAGATION DELAY:	
Measured at —2 volts level and loaded per Fig. 1	8nsec.



— Figure 1 —

POWER REQUIREMENTS:	
—12V	40ma (max.)
+6V	8ma (max.)



GDG5-20
OR GATE

KEY SLOTS PINS 27, 29

THE GDG5-20 consists of four identical three-input DC OR Gates capable of operation at frequencies from 0 to 20 MC. When one or more of the inputs are at binary "1", the output is binary "1".

DCTL (Direct Coupled Transistor Logic) is used to provide fast response times and good output drive capability. Unused inputs may be left unconnected and do not affect the operation of the unit.

OR Gates may be expanded simply by connecting the output of one gate to the input of another gate.

Due to the voltage drop across the transistors, the signal amplitude is reduced slightly as it passes through the gate. Most of this reduction occurs as the binary "1" level is shifted in the positive direction.

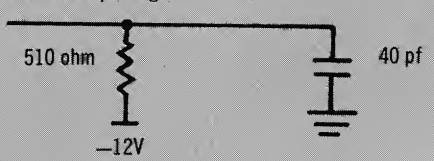
Two resistors are internally connected to the output of each gate. One or both of these may be externally connected to —12 V to provide various drive combinations.

When operating at frequencies below 10 MC, the drive capability as specified for capacitive loads may be doubled.

As in all frequency circuits, extreme care should be exercised in routing signal wires and in the grounding scheme. Signal and ground connections should be as short as possible. Ground leads should have low impedance.

SPECIFICATIONS

MODULE	20 MC
OR GATE	**GDG5-20**
INPUT:	
Frequency	0 to 20 MC
Voltage Levels	
One (—6V nominal)	—4.6 to —7.5V
Zero (0V nominal)	+1 to —1.0V
Rise Time (to produce specified outputs)	8nsec.
Input load (nominal)	4P loads
OUTPUT:	
Voltage Levels	
One (—6V nominal)	85% of Input Level
ZERO (0V nominal)	0 to —0.7V
Rise time (typical loaded per Fig. 1)	8nsec (output rise time will equal input rise time when input rise time is more than 8nsec.)
Fall Time (typical loaded per Fig. 1)	8nsec.
Typical Level Shift (output from input)	Binary One = +0.6V Binary Zero = +0.1V
Drive Capability	5N loads 20P loads 40 pf capacitance
with Resistor A connected to —12V	1.5N loads 30P loads 60 pf capacitance
with Resistor B connected to —12V	3N loads 25P loads 50 pf capacitance
with Resistors A and B both connected to —12V	0 N loads 35P loads 70 pf capacitance
PROPAGATION DELAY:	
Measured at —2 volts level and loaded per Fig. 1	8nsec.



— Figure 1 —

POWER REQUIREMENTS:	
—12V	30ma (max.)
+6V	12ma (max.)

GFF4-20
FLIP-FLOP

KEY SLOTS PINS 15, 27

The GFF4-20 consists of two identical flip-flops with internal J-K Steering designed for universal use. A gated inverter, which is common to both flip-flops, is provided at the inputs so that either a square wave or sine wave may be used as input clock signals. The square wave input has a frequency range of 0 to 20 MC while the sine wave input is limited from 5 MC to 20 MC. The circuit is triggered by a negative going signal applied to the clock input.

Set and Reset inputs are also provided for each flip-flop. These inputs are enabled by a binary 1 logic level (−6 V nominal). If a clock signal is applied when the Set input is binary 1 and the Reset input binary 0, the Set output of the flip-flop will go to the binary 1 level. If a clock signal is applied when both Set and Reset inputs are at binary 1, the flip-flop will toggle. A clock signal applied when both Set and Reset inputs are binary 0 will cause no change in the flip-flop.

The Set and Reset inputs may be used to trigger the flip-flop if the signal amplitude and rise time requirements as specified are met. For this application, the clock input should be at binary 0. Due to the internal J-K steering, a trigger signal applied to Set and Reset inputs simultaneously will cause the flip-flop to toggle.

At frequencies below 10 MC, the capability for driving capacitive loads is approximately doubled.

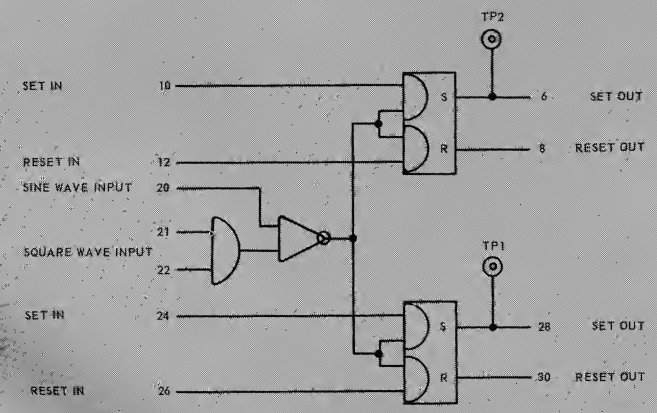
SPECIFICATIONS

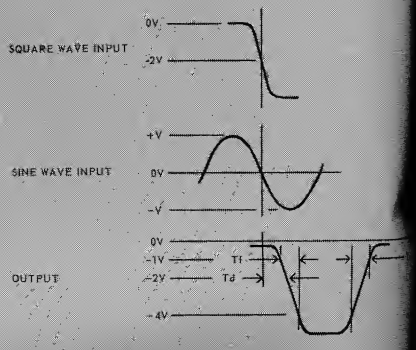
MODULE	20 MC
FLIP-FLOP	**GFF4**
INPUT	
Frequency	0 to 20 MC
Voltage Levels	
One (−6V nominal)	−4.5V to −7V
Zero (0V nominal)	+1 to −0.5V
Clock	
Sine Wave (5 to 10 MC)	8V peak to peak, min.
(10 to 20 MC)	5V peak to peak, min.
Square Wave	
Min. Amplitude	−4.5V
Min. Dwell time at Binary ZERO	20nsec.
Max. Rise Time	30nsec.
Input Load	2N loads
Set or Reset	
Min. Amplitude	−4.5V to −6V if used to trigger circuit)
Min. Dwell Time at Binary One	20nsec.
Max. Rise Time (pos. going)	15nsec. (applicable only if used to trigger circuit)
Noise Rejection, dc.	−2V
OUTPUT:	
Voltage	
One (−6.5V nominal, unloaded)	−5.0V to −8V depending on load
Zero (0V nominal)	+1 to −0.5V
Output	
Max. Rise Time (no load)	12nsec.
Max. Fall Time (no load)	12nsec.
Max. Rise Time (max. cap.)	20nsec.
PROPAGATION DELAY:	15nsec. min. 24nsec max.
Drive Capability	12N loads 5P loads 125 pf capacitance
POWER REQUIREMENTS: (per card)	
−12V	140 ma
+6V	48 ma

Note 1: The clock or trigger input is inverted before it is used as the clock, therefore the input AND gate is clocked approximately 12nsec after the clock is applied to the input.

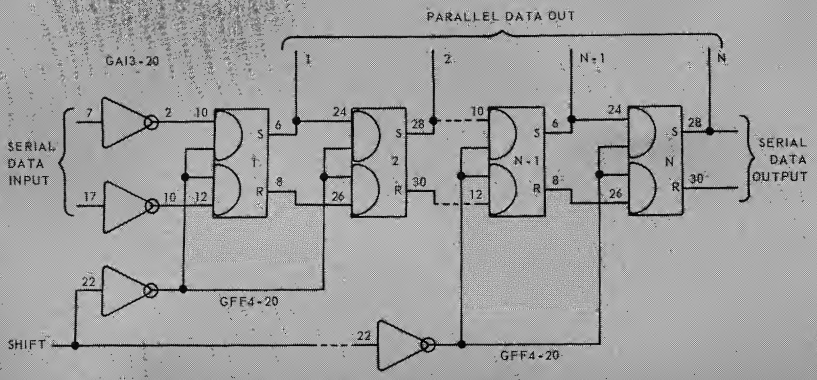
Note 2: When clock is used, connect all unused pins (20, 21 or 22) to −12V. When clock is not used, connect pin 21 to ground.

Note 3: Switching times and delay.



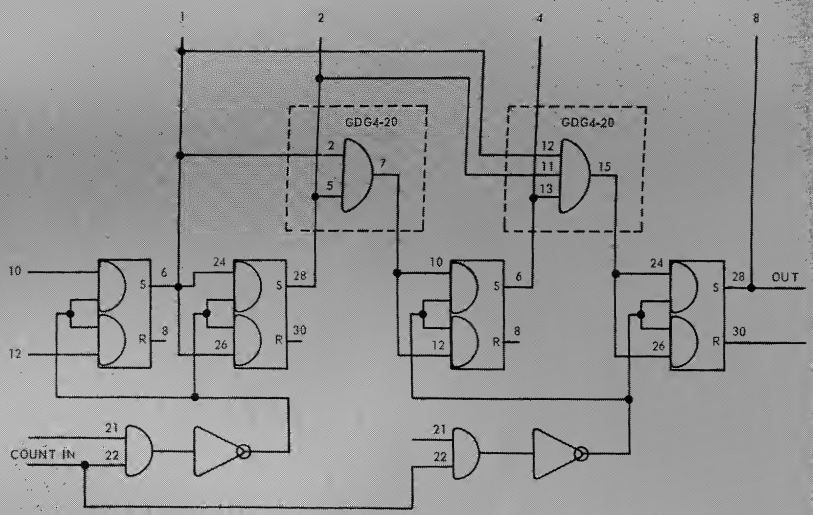


20 MC CIRCUIT APPLICATIONS

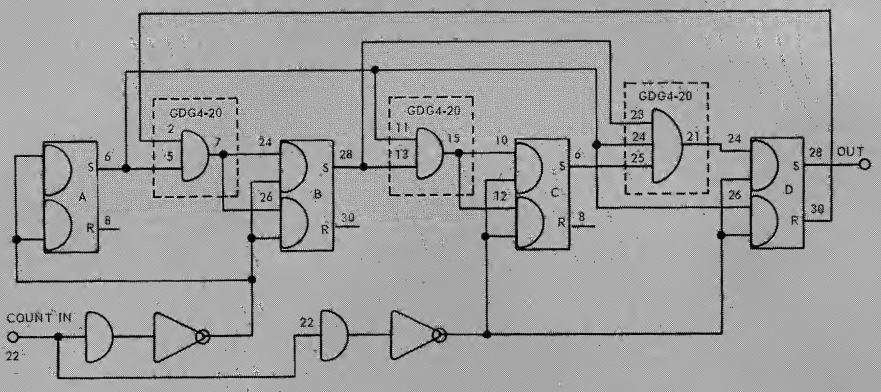


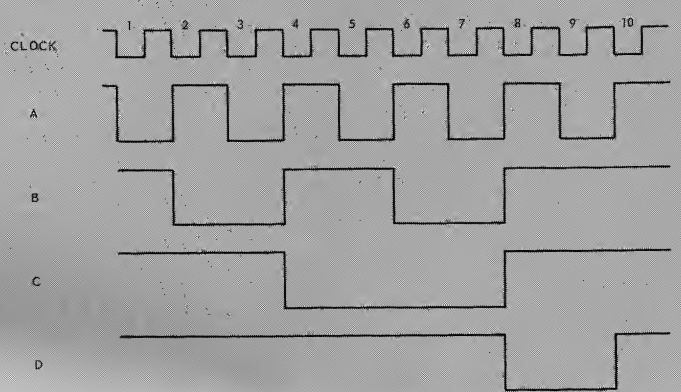
SHIFT REGISTER, 20 MC SERIAL INPUT, SERIAL OR PARALLEL OUTPUT

INVERTERS ON SERIAL INPUT NEEDED TO COMPENSATE FOR INTERNAL CLOCK DELAY. IF SERIAL DATA INPUT RATE IS 15 MC OR LESS THESE INVERTERS ARE NOT NEEDED.



20 MC BINARY COUNTER REQUIRES: 1-GDG4, 2-GFF4-20





20 MC DECADE COUNTER REQUIRES: 2-GFF4-20, 1-GDG4-20

GDA1
DIGITAL-TO-ANALOG CONVERTER

The GDA1 is an 8-bit digital-to-analog converter suitable for operation with either binary or 8-4-2-1 binary coded decimal inputs. The output is a voltage or current proportional to the magnitude of the number represented by the digital input. The voltage output with a maximum input is approximately −5 volts (one bit less than the reference voltage). The voltage output with a zero input is zero volts. The current output with a maximum input is approximately 1 milliampere (depends on reference voltage used). The current output with a zero input is zero milliamperes.

The GDA1 may also be used as two four-bit binary or binary coded decimal D to A converters. A zener reference voltage is also provided for use where requirements permit. This zener reference voltage is −5.6v ±5%, and the maximum error referred to this voltage is 2.5%.

The GDA1 may be used in the bipolar mode by supplying a positive reference of the same magnitude as the negative reference voltage. When used in the bipolar mode the output is ±1-2/3v when ±5v reference supplies are used. A precision reference voltage supply module (GRS1) for use with the GDA1 is also available.

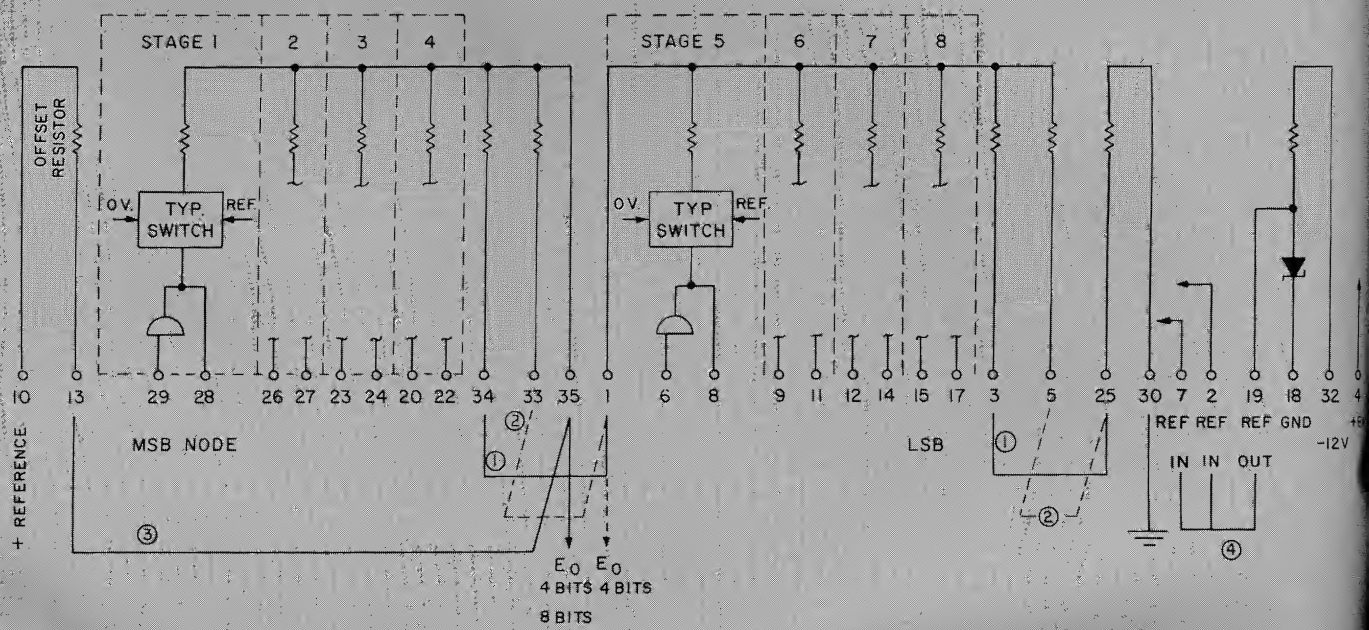
The GDA1 may be gated by means of an external diode at the gate node.

- FOR 8 BIT BINARY OPERATION - ADD JUMPERS ①
  ANALOG OUTPUT PIN 35
- FOR 8 BIT DECIMAL OPERATION (BCD) - ADD
  JUMPERS ② ANALOG OUTPUT PIN 35.
- ADD JUMPER ③ FOR BIPOLAR OPERATION.
  CAN BE USED WITH BCD OR BINARY.
- ADD JUMPER ④ WHEN USING INTERNAL ZENER REFERENCE. CAN BE USED WITH BCD OR BINARY.
- FOR HIGHER ACCURACY, USE GRS1 REFERENCE SUPPLY.
  CONNECT TO PINS 2 AND 7
- FOR TWO 4-BIT BINARY OR BCD CONVERTERS -
  GROUND PIN 34. ANALOG OUTPUT PIN 35.
  GROUND PIN 3. ANALOG OUTPUT PIN 1.

KEY SLOTS PINS 19, 31

SPECIFICATIONS

DIGITAL-TO-ANALOG CONVERTER	GDA1—.2
INPUT	
Word length	two 4-bit or one 8-bit
Frequency	0 to 200Kc
Voltage levels	
One (−10v nominal)	−9V to −12V
Zero (0V nominal)	1V to −1V
Max. Rise Time	2.5μs
Max. Fall Time	2.5μs
Input Load	4 N load (8.8 ma to neg. voltage)
Noise rejection	1.5V
OUTPUT	
Accuracy (referred to Reference voltage)	±0.15%
Voltage (depends on ref. V. used)	0 to −6V max.
Settling time to within ½ bit	3μs
Impedance	5000 ohms (Binary) 4800 ohms (BCD)
POWER REQUIREMENTS	
−12V (pin 32)	56ma
+6V (pin 4)	21ma
Gnd (pin 18)	
Reference voltage	
(AT −5V)	10ma (To neg volt)
(AT 0V)	20ma (To neg volt)



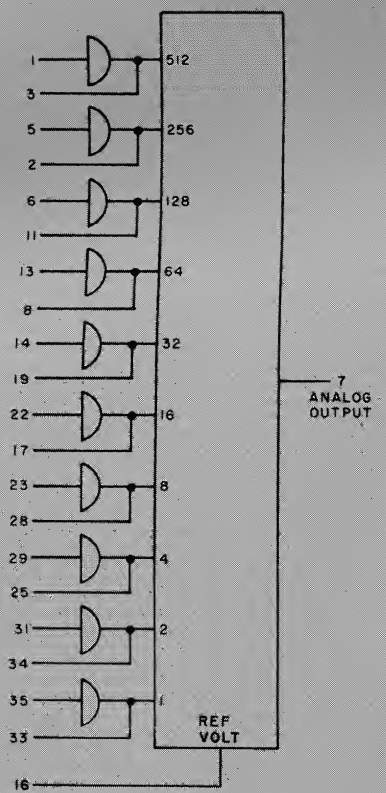
GDA2
DIGITAL-TO-ANALOG CONVERTER

KEY SLOTS PINS 25, 31

The GDA2 is a 10-bit, digital-to-analog converter. This circuit is capable of converting up to 10 bits of binary information at its inputs into an analog output voltage or current which is proportional to the magnitude of the number represented by the digital input.

The output voltage with a maximum input is approximately —5 volts (one bit less than the reference voltage). The output voltage with a zero input is zero volts. The output current with a maximum input is approximately 1 milliampere (depends on reference voltage used). The output current with a zero input is zero milliamperes.

The GDA2 may be gated by means of an external diode at the gate node.



SPECIFICATIONS

DIGITAL-TO-ANALOG CONVERTER	GDA2-.2
INPUT	
Word length	10 bits
Frequency	0 to 200KC
Voltage levels	
One (—10V nominal)	—9V to —12V
Zero (0v nominal)	+1V to —1V
Maximum Rise Time	2.5μs
Maximum Fall Time	2.5μs
Input Load (Logic Input)	4 N loads (8.8ma to neg voltage)
Reference Voltage	0V to —6V
OUTPUT	
Accuracy (referred to Reference Voltage)	±0.12%
Voltage (depends on ref. V used)	0 to —6V max.
Settling time to within ½ bit	3μsec
Impedance	5000 Ohms
POWER REQUIREMENTS	
—12V (pin 32)	88ma
+6V (pin 4)	26ma
Gnd (pin 18)	
Reference voltage (0V to —6V)	12ma

GRS1
REFERENCE VOLTAGE SUPPLY

The GRS1 is a reference voltage supply module for use with digital-to-analog converter modules when extreme accuracy is required. The GRS1 reference supply is basically a self-regulating circuit which generates and automatically regulates a precise −5 volt output from standard −12V and +6 volt inputs.

The GRS1 can drive up to 20 GDA1s and has a maximum output of 200 milliamps.

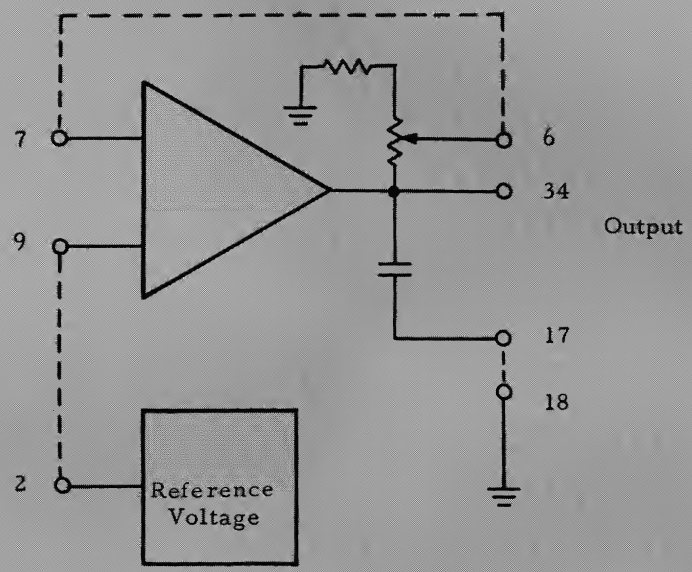
The GRS1 may be slaved to its own highly stable, temperature compensated zener reference diode, or it may be slaved to an external reference.

When used as a slaved reference supply, the linear output range is −2.0 volts to −9.0 volts. Slew rate is 0.35 volts/μsec.

KEY SLOTS PINS 23, 25

SPECIFICATIONS

REFERENCE VOLTAGE SUPPLY	GRS1
OUTPUT	
Voltage	Adjustable to −5V
Drive Capability	20 GDA1s or 200 milliamps to a negative voltage (10ma per GDA1)
Stability:	
Temperature	±.003%/°C
Load	.0005%/ma
Power Supply (±2.5%)	.01%
Power Supply (±5%)	.02%
Noise (Typical) No Load to Full Load	.3mv, peak
Response Time (Typical)	1μs
POWER REQUIREMENTS:	
−12VDC (pin 32)	250ma
+6VDC (pin 4)	18ma
Gnd (pin 18)	



NOTE: Dash lines indicate external jumper wires.

TYPICAL APPLICATION

8 GDA1-.2 channels operating over temperature range of 25 ±5°C with power supply variation of ±2.5%.

Temperature	5 x .003%	= .015%
Load	80 x .0005%	= .040%
Power Supply	at ±2.5%	= .010%
Total Maximum Error of GRS1		± .065%

GVC1
VOLTAGE COMPARATOR

KEY SLOTS PINS 32, 34

The GVC1 Voltage Comparator is an ultra-stable, high-speed comparison circuit which provides a binary 0 (0 v.) or binary 1 (−10 v. nominal) output, respectively, for an analog input voltage above or below the threshold voltage (switching point).

The unit consists of a differential amplifier, connected in an operational configuration, driving a differential Schmitt Trigger. The input transistors in the differential amplifier are mounted on the same silicon chip, providing excellent tracking and temperature characteristics. Typical hysteresis is less than 2 millivolts.

Feedback in the amplifier is non-linear, providing fast recovery from large signal transients.

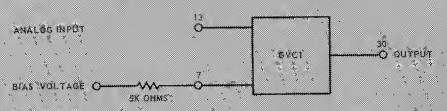
A common problem in voltage comparator and differential amplifier circuits is the "hunting" and oscillation that occurs when the circuit is at the switching point. The GVC1 has a unique feature incorporating positive feedback around the Schmitt Trigger circuit which virtually eliminates this problem.

The GVC1 may be used with the GDA2-.2 digital-to-analog converter card, GRS1 reference supply and standard Raytheon Computer flip-flop and gate circuits to make a 10-bit successive approximation analog-to-digital converter with an 8KC word conversion rate. (Contact Raytheon Computer for complete block and wiring diagrams.)

The GVC1 utilizes the −5 v. source from the GRS1 reference supply to generate internally a highly accurate and stable −2 v. at one input of the differential amplifier. The other input to the amplifier is the sum of the analog voltage on pin 13 through an internal 20K resistor and the voltage on the direct input (Pin 7) through an external 5K resistor. This approach to voltage comparison offers several advantages.

1) The analog voltage input covers the ±10 v. range meeting most requirements.
2) The direct input covers the 0 to −5 v. range from a 5K source which is precisely the output of the GDA1-.2 and the GDA2-.2 digital-to-analog converter modules. Therefore, the output of these D/A modules may be connected directly to the GVC1, creating a high-speed digitally-controlled voltage comparator with accuracy to 10 binary bits or 3 decimal digits.

To use the GVC1 voltage comparator as a general purpose comparator, connect as shown. The switching point (threshold voltage) may be any voltage between +10 volts and −10 volts.



The formula for determining the external bias voltage is:

$$\text{Bias Voltage} = -\left(\frac{\text{Threshold Voltage}}{4} + 2.5\right)$$

For example, if it is desired to set the switching point at +8.0 volts, the bias voltage is:

$$\text{Bias Voltage} = -\left(\frac{+8.0\text{ v.}}{4} + 2.5\right) = -4.5\text{ volts}$$

As the analog voltage varies above or below +8.0 volts, the GVC1 output will be 0 volts or −12 volts respectively.

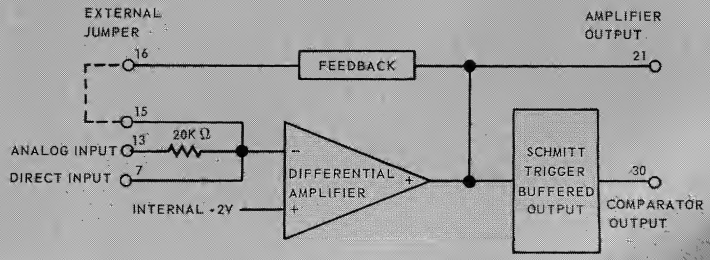
The bias voltage will always be between 0 volts and −5.0 volts.

For maximum accuracy, the analog voltage source should have as low an output impedance as possible.

SPECIFICATIONS

VOLTAGE COMPARATOR	GVC1
Analog Input (Pin 13)	
Range	±10 volts
Impedance	20 K ohms
Driving Source Impedance	2 ohms for comparison accuracy of 0.1% under worst case conditions
Direct Input (Pin 7)	
Range	0 v. to −5 v.
Impedance	Greater than 100 megohms
Driving source impedance	5000 ohms ±0.02% for comparison accuracy of 0.1% under worst case conditions
Comparator Output (Pin 30)	
Binary 1 (−10 v. nominal)	−9 v. to −12 v
Binary 0 (0 v. nominal)	0 v. to −0.3 v.
Max. Rise Time (Full Load)	1.0 μs
Drive Capability	10 N loads 10 P loads 2 C2 loads
Settling Time (from input change to corresponding output change)	
For large signal input When used in successive approx. A/D allow 8 μs per bit for overall conversion time	6 μs max.
Comparator error considerations	
Offset	40 ppm/°C
Linearity	20 ppm/°C
Gain Stability	20 ppm/°C
Amplifier	
Closed loop gain	26 db at DC
Bandwidth	3.5 mc at 0 db rolled off at −6 db/octave
Common Mode Rejection	−100 db at 100 cps
POWER REQUIREMENTS	
−12V (Pin 32)	60 ma
+6V (Pin 34)	30 ma
−5V (Reference voltage as from GRS1) (Pin 23)	10 ma
Digital GND. (Pin 18)	
Analog GND. (Pin 17)	

NOTE: The +6 v. power is connected to pin 34 on the GVC1, not pin 4 as for all other standard Raytheon Computer modules. This puts all digital power on one side of the board away from the analog circuitry and keeps the analog summing junction relatively free of digital noise.



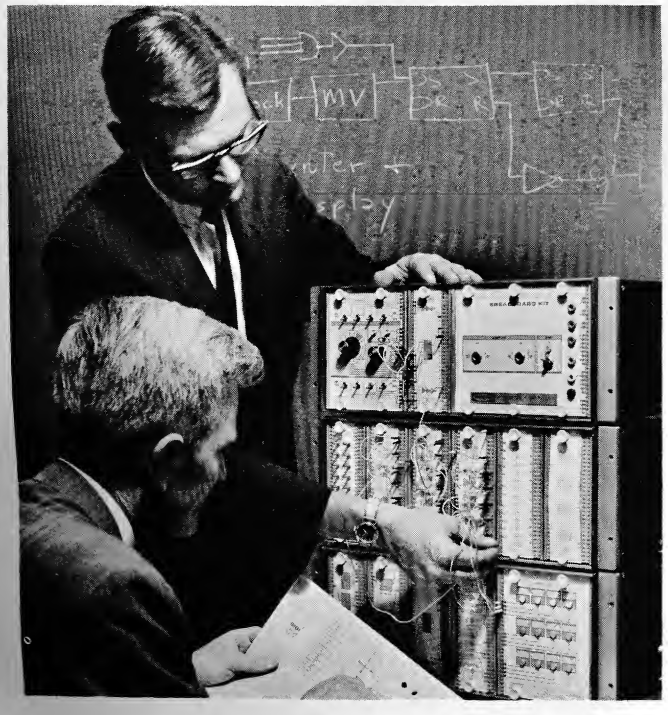
the fastest, most convenient, most economical way to design, demonstrate, checkout and test digital circuits.

DIGITAL MODULE BREADBOARD AND TRAINING KIT

Raytheon Computer's Digital Module Breadboard and Training Kit, designated the MBK1, enables logic designers, electronic system engineers, and electronic engineering instructors to quickly and easily design and test digital logic circuits operating up to 5MC frequencies. Using this Breadboard Kit, an engineer can connect a series of Raytheon Computer germanium digital logic modules in experimental or test circuit arrangements, or for digital assembly breadboards, system simulation, or classroom instruction without soldering connections or use of an oscilloscope. The Breadboard Kit can also be used to checkout small systems and sub-systems of larger digital complexes.

COMPACT SELF-CONTAINED UNIT

The self-contained portable or rack-mounted Breadboard Kit includes an indicator panel, signal generator, power supply, breadboard chassis and module adapters. Also included are patchcords, logic symbol cards and up to twenty-five 200KC, 1MC, and 5MC circuit modules. Movable breadboard grip handles can be vertically positioned for rack mounting or horizontally positioned for portable bench top work. Additional chassis increments and adapters are available for expanded Breadboard Kits.



EASY TO USE

The modules are plugged into adapters which are then inserted in the Breadboard Kit chassis. Symbol cards on the adapters indicate input and output connections. Module interconnections are made by patching card-to-card (with patchcords supplied) for desired logic combination. As many as ten circuit modules can be connected and operated simultaneously with the standard Breadboard Kit. Systems may be originated, changed or taken down at the designer's will. The MBK1 Breadboard Kit enables logic designs to be analyzed without soldering, or waste of costly engineering time and materials.

DYNAMIC OR STATIC CIRCUIT ANALYSIS

The Breadboard Kit provides both dynamic and static circuit analysis. Frequency analysis from 1 pps to 5MC uses an integral clock; a manual clock provides single pulse operation for static analysis. Indicator panel lights provide direct observation of circuit operation.

BREADBOARD KIT AVAILABLE IN THREE MODELS

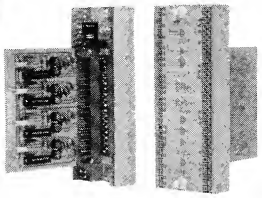
Basic Model: MBK1-04 is a basic Breadboard Kit primarily for users who have a full array of Raytheon Computer modules in stock. This kit consists of 3 chassis, power supply, indicator panel, signal generator, component panel, power harness, jumper kit, and 10 adapters.

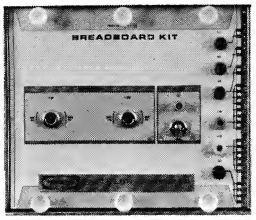
Standard Model: Model MBK1-07 is primarily used for general purpose operation at 200 KC. It can be used in the laboratory and for classroom instruction. This model consists of a basic kit plus 16 symbol cards and the following modules:

1	GA12 Amplifier Inverter	12 circuits
2	GDG3 OR Gates	10 circuits
2	GDG2 AND Gates	16 circuits
1	GEF1 Emitter Follower	12 circuits
3	GFF3 Flip-Flops	12 circuits
1	GMV1 Multivibrator Clock	1 circuit
1	GOS3 One-Shot	3 circuits
2	GUL1 Universal Logic	20 circuits
2	GSR3 Shift Registers	6 circuits
1	GNA1 NAND Gate	6 circuits
1	GDG6 AND/OR Gate	6 circuits
	TOTAL CIRCUTS	101

DIGITAL MODULE BREADBOARD - TRAINING KIT

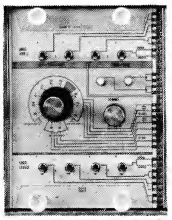
the fastest, most convenient, most economical way to design, demonstrate, checkout and test digital circuits.

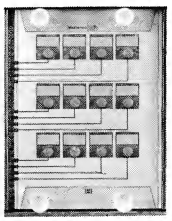

MODULE ADAPTER

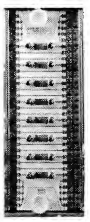


POWER SUPPLY

SYMBOL CARD


SIGNAL GENERATOR PANEL


INDICATOR PANEL


COMPONENT PANEL

Expanded Model: An expanded Breadboard Kit—MBK1-08 with 26 modules is designed for general purpose operation, counting control, and data handling applications in the 200 KC frequency class. A basic kit plus 1 extra chassis, 6 extra adapters, 1 extra jumper kit, 26 symbol cards, and the following modules comprise the MBK1-08.

1	GAI2 Amplifier Inverter	12 circuits
1	GEF1 Emitter Follower	12 circuits
1	GMV1 Multivibrator Clock	1 circuit
1	GOS3 One-Shot	3 circuits
4	GFF3 Flip-Flops	16 circuits
2	GDG2 AND Gates	16 circuits
2	GDG3 OR Gates	10 circuits
1	GDG6 AND/OR Gate	6 circuits
3	GUL1 Universal Logic	30 circuits
4	GHA1 Half Adders	16 circuits
2	GNA1 NAND Gates	12 circuits
4	GSR3 Shift Registers	12 circuits
2	GSR2 Shift Registers	4 circuits
	TOTAL CIRCUITS	150

BREADBOARD KITS READILY EXPANDED

A Breadboard Kit can be readily expanded by ordering additional chassis sections. Each section can hold six modules or additional power supply or signal generators as desired.

SPECIFICATIONS

MBK1 Breadboard Kit

Weight (Basic Kit)	50 pounds
Height	21 inches
Width	19 inches
Depth	9 inches
Power Requirements	110 Volts a-c

MODULE ADAPTERS

Module adapters are equipped with permanent 35-pin connectors. Plastic symbol cards corresponding to specific circuits attach to the outside adapter face. Symbol cards indicate module input and output points. Single input jacks are on left side of adapter; double output jacks on right. Adapter with module plugged in is securely installed in the Breadboard Kit by means of nylatch fasteners. The additional row of jacks on the right or output side of each adapter simplifies circuit wiring and circuit output monitoring.

POWER SUPPLY

Power Supply unit — BPS1 — provides −12 volts at 2 amps and a +6 volts 375 ma dc output. Power supply or modules cannot be damaged by output shorting or overloading. Voltages are adjustable by screwdriver over a 10% range. The Power Supply has an integral a-c power cable leading from the chassis to external source.

MODULE SYMBOL CARDS

Plastic symbol cards are available for each Raytheon Computer digital module and carry module designation (e.g., GFF1), module logic diagrams, input-output designations and pin numbers. Symbol cards are easily removed and replaced on adapters to match modules being breadboarded. Blank symbol cards are available for sketching in special or test circuit logic diagrams.

SIGNAL GENERATOR PANEL

Signal Generator Panel — BSG1 — generates clock signals at frequencies from 1 pps to 5MC. Frequencies up to 1MC use appropriate multivibrator modules; frequencies from 1MC to 5MC use a 5MC clock generator circuit card. A coarse adjustment switch is provided for frequency changes in steps from 1 pps to 5MC. For continuous frequency adjustment from 0 to 1MC a Vernier Control is provided. Two push buttons actuate manual clocks which transmit signal pulses for manual operation of a system. Eight switches provide static logic levels; binary 1 = −12 volts; binary 0 = 0 volts. The switches are also useful for static checkout of dc logic or providing logic levels for parallel transfer into registers, etc.

INDICATOR PANEL

Three rows of lights (four lights to a row) on the indicator panel provide direct indication of circuit conditions. To observe the state of a circuit, the output is connected to the indicator panel. If indicator lights are *on*, the circuit is at *logic* 1; if indicator lights are *off*, the circuit is at *logic* 0.

COMPONENT PANEL

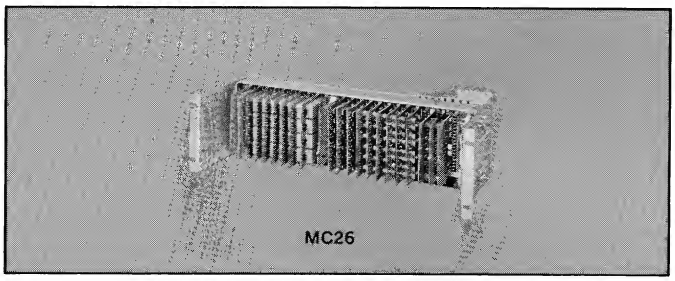
The Component Panel is used when capacitors or resistors are required to adjust pulse width of one-shots, for loading gates, or any logic circuit. The panel also provides internally jumpered jacks if larger fan-out jacks are required. Eight sets of external mounting studs hold the components. Studs are connected to jacks for output connections.

RAYTHEON

DIGITAL MODULE ACCESSORY EQUIPMENT

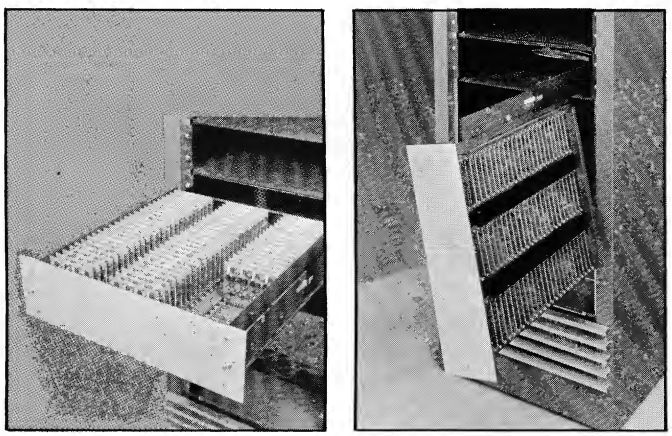
Adds convenience and usefulness to Raytheon Computer modules...

Raytheon Computer has available a complete array of module accessory equipment which meets practically all digital circuit and system development, test, checkout and final assembly requirements. Module accessory equipment and tooling includes: module cases, power supplies, connectors, indicator panels, blank cards, extender and utility boards, connector installation and extractor tools, and module card extractors. All module accessory equipment can be used with either germanium or silicon modules with the exception of module case front panels.



MC26 MODULE CASE

MC26 module case is suitable for both systems and breadboard use. This low cost unit can accommodate up to 26 standard modules. Circuit cards may be connected either from the front or back for maximum accessibility to connector pins. The case requires 5¼" of panel height in a standard 19" rack and is less than 8" deep.



MCR75—side hinge tilt down feature allows easy connector and module access.

MCR75 MODULE CASES

MCR75 Module Cases—hold up to 75 Raytheon Computer standard digital modules. Cases are suitable for mounting in standard 19 inch racks. Two models are offered: MCR75-500 series—accommodates solder tail connectors with 5¼" front panel; MCR75-700 series—uses solder tail, wire wrap, or taper pin connectors and has a 7" front panel.

Double case slides allow smooth sliding in or out of rack. Safety lockout mechanism prevents case from being accidentally slid into rack while modules are being tested. Side hinge tilt-down feature provides easy access for connector soldering and module trouble shooting. Power cables pass between horizontally positioned rollers. This prevents cable wear and tear when sliding case in and out. Optional rear panel is offered with holes to accommodate 50-pin Amphenol or Cannon connectors.

MCR75 BASIC MODULE CASES

MCR75-500—basic 5¼" case with blank connector mounting panel.

MCR75-517—basic 5¼" case including 17 Amperex indicators.

MCR75-560—basic 5¼" case including 60 Amperex indicators.

MCR75-700—basic 7" case

MCR75-717—basic 7" case including 17 Amperex indicators.

MCR75-760—basic 7" case including 60 Amperex indicators.

MCR75-001—Connector mounting panel for mounting eight 50-pin connectors.

MCR75-002—50-pin male plug for use with MCR75-001.

MCR75-003—50-pin female receptacle for use with MCR-75-001.

POWER SUPPLIES

Power Supplies—MPS20, MPS21, MPS22—featured here are designed for use with Raytheon Computer germanium modules. These solid state, convection cooled units furnish 12 volt DC and 6 volt DC power requirements for various module mounting cases. One unit—MPS22—includes 50 volt DC and 1 volt AC (rms) power for Amperex indicators. Ripple voltage does not exceed 150 millivolts peak to peak. Power Supplies are designed for continuous duty operating under full load conditions.

The output of all DC power supplies is supplied by transformer coupling and full-wave rectification. All outputs are floating and may be referenced for either output polarity.

MODULE POWER SUPPLIES SPECIFICATIONS:

MPS20—*For use with MC 26 module case.*

Power Capabilities

12 volt DC output (regulated) at	1.5 amps
Load change	10.0%
Line change	2.5%
On-off overshoot	20%
6 volt DC output (regulated) at	0.375 amps.
Load change	10.0%
Line change	2.5%
On-off overshoot	20%
Operating temperature range	+5°C to +45°C.
Weight	(approx.) 15 lbs.
Dimensions	17" x 5" x 5"

MPS21—*Rack mounting 5¼" high front panel for use with the MCR75 module case.*

Power Capabilities

12 volt DC output (regulated) at	5.0 amps.
Load change	10.0%
Line change	2.5%
On-off overshoot	20%
6 volt DC output (regulated) at	1.25 amps.
Load change	10.0%
Line change	2.5%
On-off overshoot	20%
Operating temperature range	+5°C to +45°C.
Weight	(approx.) 25 lbs.
Dimensions	19" x 9" x 5"

MPS22—*Rack mounting 5¼" high front panel—with power for Amperex indicators—for use with MCR75 module case.*

Power Capabilities

12 volt DC output (regulated) at	5.0 amps.
6 volt DC output (regulated) at	1.25 amps.
50 volt DC (unregulated) at	.050 amps.
1 volt AC (unregulated) at	1.8 amps.
Load change	10.0%
Line change	2.5%
On-off overshoot	20%
Weight	(approx.) 25 lbs.
Dimensions	19" x 9" x 5"
Operating temperature range	+5°C to +45°C

BLANK CIRCUIT BOARD

MBB1 35 pin Blank Board is a standard size 3¾" x 4¼" card for special or experimental circuit construction.

EXTENDER BOARDS

The XT100 Extender Boards provide circuit continuity for trouble shooting under operating conditions. A standard module is plugged into the XT100 which is then inserted into the module's designated connector. This permits the circuit card to extend approximately 5 inches beyond the other cards in a case.

MODULE CARD EXTRACTOR

Model MCE1 module card extractor grips circuit card edges for smooth withdrawal of card from case and connector.

MUB1 MODULE UTILITY BOARD

Experimental digital circuits may be constructed with the 35-pin MUB1 module utility board. Printed grid on front side and letter/number system is used as an aid in circuit construction. Holes provide mounting for up to 16 transistors, plus capacitors, resistors or diodes on card. For identification, name and number of particular assembly can be rubber stamped in areas at top of board. All 35 pins are hand soldered and interconnect to copper printed circuits.

CONNECTORS

To fit every module assembly need three types of connectors are offered. These connectors give simple and positive performance which assure uniformity of retention, resulting in excellent electrical stability and reliability. All connectors are 35-pin, standard—3½" long—and compatible with Raytheon Computer's module line. Connector module guides prevent card damage during insertion or removal.

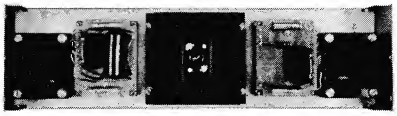
VS100 VS100 is a solder tail female connector. 24, 22, and 20 gauge wire can be applied to this connector. All mounting hardware and keying pins are included.

VW100 Wire wrap connector VW100 is designed for simple time-saving patch cord and wire assembly. It accepts up to 18 gauge wire. All mounting hardware and keying pins are included.

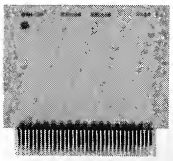
VT100 Taper pin connector VT100 features sockets at both ends. This allows positive connection which permits use of patch cords and easy wiring changes without soldering. Sockets are numbered for easy identification during troubleshooting. All mounting hardware and keying pins are included.

DIGITAL MODULE APPLICATION MANUAL

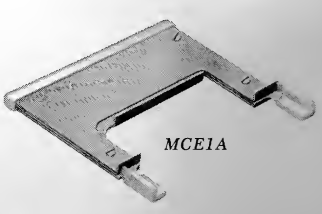
As a customer service Raytheon Computer offers design assistance in the use of digital logic modules. A Digital Module Application Manual - SP175 - is available which offers assistance for basic circuit design, an introduction to logic symbology, and a discussion of digital system design criteria. In addition, Raytheon Computer circuit card descriptions, loading considerations, and rules of module applications are given in full detail. This manual may be obtained by writing Raytheon Computer: price $1.50.



MPS20

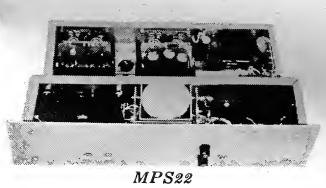


MBB1

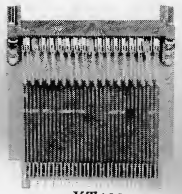


MCE1A

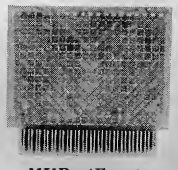
VT100



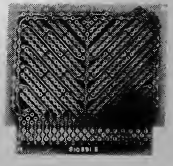
MPS22



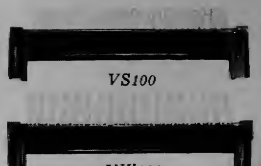
XT100



MUB1 (Front)



MUB1 (Back)



VS100

VW100

1 MC MODULES

Model No.	Catalog No.	Description	Quantity Discount 1 to 10	11 to 25	26 to 100	101 to 200
GAI2-1	515793	Amplifier Inverter (12 circuits)	$ 66.00	64.00	62.05	60.70
GBC1-1	515425	Binary Counter	63.00	61.10	59.20	57.95
GCG1-1	515328	Clock Generator, free running	85.00	82.45	79.90	78.20
GCG2-1	515339	Clock Generator, crystal-controlled 200 kc to 1 mc (specify frequency)	105.00	101.85	98.70	96.60
GDC1-1	515365	Decade Counter (8-4-2-1 Code out)	65.00	63.05	61.10	59.80
GDG2-1	515475	Diode AND Gate (20 inputs, 6 outputs)	25.00	24.25	23.50	23.00
GDG3-1	516336	Diode OR Gate (21 inputs, 5 outputs, level restoring)	60.00	58.20	56.40	55.20
GDI1-1	515394	Driver Inverter (10 circuits)	83.00	80.50	78.00	76.35
GDI2-1	515386	Driver Inverter (10 circuits, cable driver)	80.00	77.60	75.20	73.60
GDL1-1	517224	Delay Line, Magnetostrictive, to 1300 μ sec	425.00	412.25	399.50	391.00
GDM1-1	515596	Decoder Matrix - Binary to octal or decimal	64.00	62.10	60.15	58.90
GEF1-1	515375	Emitter-Follower (12 circuits)	68.00	65.95	63.90	62.55
GFF1-1	515454	Flip-Flop (4 circuits, universal)	65.00	63.05	61.10	59.80
GFF2-1	515436	Flip-Flop (4 circuits) RS	52.00	50.45	48.90	47.85
GFF3-1	517156	Flip-Flop, Gated (4 circuits)	69.00	66.95	64.85	63.50
GHA1-1	517230	Half Adder, Subtractor, Comparator (4 circuits)	85.00	82.45	79.90	78.20
GIG1-1	515407	Input Gate (Pulse OR Gate, 22 inputs, 10 outputs)	38.00	36.85	35.70	34.95
GLA1-1	517235	Linear Amplifier, Gain 90, 20 cps to 1 MC(2)	60.00	58.20	56.40	55.20
GMV1-1	515372	Multivibrator Clock (with gated drivers)	82.00	79.55	77.10	75.45
GNA1-1	515593	NAND Gate (16 inputs, 6 outputs)	50.00	48.50	47.00	46.00
GOS3-1	516346	One-Shot (3 circuits)	80.00	77.60	75.20	73.60
GRG1-1	515401	Reset Gate (4 circuits, 6 outputs per circuit)	38.00	36.85	35.75	34.95
GSR2-1	515486	Bidirectional Shift Register (2 circuits)	68.00	65.95	63.90	62.55
GSR3-1	516356	Bidirectional Shift Register (3 circuits)	80.00	77.60	75.20	73.60
GSR4-1	517314	Shift Register, Serial, Parallel	65.00	63.05	61.10	59.80
GST1-1	515466	Schmitt Trigger (4 circuits)	78.00	75.65	63.30	71.75
GST2-1	515460	Schmitt Trigger (2 circuits, adjustable threshold)	70.00	67.90	65.80	64.40
GUL1-1	517561	Universal Logic (18 Gate inputs, 4 Inverters)	37.00	35.90	34.80	34.05
GLC7-1	518659	Level Converter (RC to IBM current mode C level)	95.00	92.15	89.30	87.40
GLC8-1	518655	Level Converter (IBM mode C levels to RC)	53.00	51.40	49.80	48.75
GLC9-1	517199	Level Converter	90.00	87.30	84.60	82.80

5 MC MODULES

GBC1-5	515421	Binary Counter (4 circuits)	82.00	79.55	77.10	75.45
GCG1-5	515153	Clock Generator, free running	95.00	92.15	89.30	87.40
GCG2-5	515331	Clock Generator, crystal-controlled 1 mc to 5 mc (specify frequency)	115.00	111.55	108.10	105.80
GDC1-5	515369	Decade Counter (8-4-2-1 Code out)	85.00	82.45	79.90	78.20
GDG2-5	515472	Diode AND Gate (20 inputs, 8 outputs)	43.00	41.70	40.40	39.55
GDG3-5	516339	Diode OR Gate (21 inputs, 5 outputs, level restoring)	80.00	77.60	75.20	73.60
GDI1-5	515398	Driver Inverter (10 circuits)	110.00	106.70	103.40	101.20
GDI2-5	515079	Driver Inverter (10 circuits, cable driver)	100.00	97.00	94.00	92.00
GDM1-5	515599	Decoder Matrix - Binary to octal or decimal	75.00	72.75	70.50	69.00
GEF1-5	515378	Emitter-Follower (12 circuits)	95.00	92.15	89.30	87.40
GFF1-5	515449	Flip-Flop (4 circuits, universal)	85.00	82.45	79.90	78.20
GFF2-5	515432	Flip-Flop (4 circuits) RS	59.00	57.25	55.45	54.30
GFF3-5	517332	Flip-Flop, Gated (4 circuits)	90.00	87.30	84.60	82.80
GHA1-5	517323	Half Adder, Subtractor, Comparator (4 circuits)	95.00	92.15	89.30	87.40
GIG1-5	515094	Input Gate (Pulse OR Gate, 22 inputs, 10 outputs)	59.00	55.30	53.60	52.45
GLC9-5	517187	Level Converter	105.00	101.85	98.10	96.60
GNA1-5	515708	NAND Gate (16 inputs, 6 outputs)	65.00	63.05	61.10	59.80
GOS3-5	516349	One-Shot (3 circuits)	95.00	92.15	89.30	82.80
GRG1-5	515404	Reset Gate (4 circuits, 6 outputs per circuit)	57.00	55.30	53.60	52.45
GSR2-5	515484	Bidirectional Shift Register (2 circuits)	85.00	82.45	79.90	78.10
GSR3-5	516359	Bidirectional Shift Register (3 circuits)	100.00	97.00	94.00	92.00
GSR4-5	517317	Shift Register, Serial, Parallel	85.00	82.45	79.90	78.10
GST1-5	515469	Schmitt Trigger (4 circuits)	90.00	87.30	84.60	82.80
GST2-5	515457	Schmitt Trigger (2 circuits, adjustable threshold)	80.00	77.60	75.20	73.60
GUL1-5	517563	Universal Logic (18 Gate inputs, 4 Inverters)	49.00	47.55	46.05	45.10

20 MC MODULES

GAI3-20	517753	Four 20 mc Inverters	120.00	116.40	112.90	109.50
GDG4-20	517794	Four 3-input AND Gates, 20 mc	135.00	130.95	126.90	124.20
GDG5-20	517774	Four 3-input OR Gates, 20 mc	120.00	116.40	112.90	109.50
GFF4-20	517302	Two 20 mc Flip-Flops. Each input has two input AND Gates. There is a common clock input for two Flip-Flops. This clock input is gated with a 2-input AND Gate and will accept sine wave signals from 5 to 20 mc.	130.00	126.10	122.35	118.65

MODULE ACCESSORIES

Model No.	Catalog No.	Description	Unit Selling Price
GIL1	530480	Indicator light	$ 11.00
GIL2	530493	Switch, Indicator Light	12.00
IT 1	506684	Basic Insertion Tool, taper pin.	23.70
IT 2	506685	Pull Test Insertion Tool, taper pin.	38.20
IT 3	506686	Captive and Pull Test Insertion Tool.	46.50
IT 4	506687	Installation Tool (for crimping wire, taper pin).	40.50
IT 5	506688	Wire Wrap Tool for 24-Gage Wire with Insulation Stripper	82.50
IT 6	506689	Wire Unwrapper.	6.40
MCE1A	530587	Card Extractor.	20.00
MC26	507075	Module Case. Holds 24 module cards, 5¼'' high.	40.00
MCR-75-500	511115-001	Module case with 5¼'' blank front panel. Holds 75 modules. For solder tail connectors only.	250.00
MCR-75-517	511115-005	Module case with 5¼'' panel and 17 Amperex indicators. Holds 75 modules. For solder tail connectors only.	395.00
MCR-75-560	511115-009	Module case with 5¼'' panel and 60 Amperex indicators. Holds 75 modules. For solder tail connectors only.	685.00
MCR-75-700	511115-013	Module case with 7'' blank front panel. Holds 75 modules. For solder tail, wire wrap or taper pin connectors.	250.00
MCR-75-717	511115-017	Module case with 7'' panel and 17 Amperex indicators. Holds 75 modules. For solder tail, wire wrap or taper pin connectors.	395.00
MCR-75-760	511115-021	Module case with 7'' panel and 60 Amperex indicators. Holds 75 modules. For solder tail, wire wrap or taper pin connectors.	685.00
MCR-75-001	511098	Connector mounting panel with 8 connector mounting holes for mounting 50-pin miniature Cannon connectors (Cannon #DDM-50) see MCR-75-002/003. Will fit any MCR-75 module case.	15.00
MCR-75-002	503589-001	Male plug 50-pin, 5 amp solder pot contacts accept #20 wire. For use with MCR-75-001 panel. (Cannon No. DDM50P)	15.00
MCR-75-003	503589-002	Female receptacle 50-pin, 5 amp solder pot contacts accept #20 wire. For use with MCR-75-001 panel. (Cannon No. DDM50S)	16.90
MCR-75-005	530008	Chassis mounted connector locking device. For use with chassis connector MCR-75-002 and MCR-75-003.	2.00
MCR-75-006	517420-005	Female cable plug 50 pin 5 amp solder pot contacts accept #20 wire (mates with MCR-75-002). Includes cable clamp and locking device.	29.00
MCR-75-007	517420-001	Male cable plug 50 pin 5 amp solder pot contacts accept #20 wire (mates with MCR-75-003). Includes cable clamp and locking device.	23.00
MPS20	515144	Power Supply. ± 12 v at 1.5 amps; ± 6 v at 0.375 amps; Mounts on back of MC26.	285.00
MPS21	515145	Power Supply. ± 12 v at 5.0 amps; ± 6 v at 1.25 amps; 5¼'' high, for rack-mounting.	400.00
MPS22	515146	Power Supply. ± 12 v at 5.0 amps; ± 6 v at 1.25 amps; ± 50 v at 0.05 amps; 1 v AC at 1.8 amps; 5¼'' high; suitable for rack-mounting. Has power for Amperex indicators.	450.00

BLANK BOARDS, EXTENDER BOARDS, CONNECTORS

Model No.	Catalog No.	Description	Quantity Discount 1 to 10	11 to 25	26 to 100	101 to 200	201 to 500
MBB1	516362	Blank Circuit Board 3¾'' x 4¼''	$16.00	15.50	15.05	14.70	14.40
VS100	506238	Solder tail female connector 35-pin	4.00	3.90	3.75	3.70	3.60
VT100	506239	Taper pin female connector, 35-pin	5.25	5.05	4.95	4.85	4.75
VW100	506446	Wire wrap connector, 35-pin	4.00	3.90	3.75	3.70	3.60
XT100	505774	Extender Board, 35-pin	41.00	39.80	38.60	37.80	37.00
MUB1	515162	Utility Board with etched circuitry for general purpose use 3¾'' x 4¼''	21.00	20.35	19.75	19.30	18.90

MBK1 MODULE BREADBOARD KIT

MBK1-04		Basic Breadboard Kit without modules	$ 1,300.00
MBK1-07		Breadboard Kit with 17 modules for general purpose digital systems development, instruction and demonstration. 200 kc operation.	2,074.00
MBK1-08		Expanded Breadboard Kit with 28 modules for general purpose digital systems development.	3,014.00
MBKO-01	515063	Breadboard Chassis	99.00
MBKO-02	515099	Adapter	30.00
MBKO-03	516376	Jumper Kit - 150 Jumpers (3 sizes, 3 colors)	90.00
MBKO-04	515533	Power Harness	6.00
BPS1-01	515100	Power Supply	322.00
BSG1-01	515118	Signal Generator	160.00
BCP1-01	515110	Component Panel	43.00
BIP1-01	515108	Indicator Panel (without module)	82.00
MBKO/xxx		Symbol Card (Specify module, e.g., MBKO/GFF1)	1.00

CONTACT COMPANY OR SALES REPRESENTATIVE FOR INFORMATION ON VOLUME AND LARGE QUANTITY DISCOUNTS.

PRICES SUBJECT TO CHANGE WITHOUT NOTICE AND SUBJECT TO STATE AND LOCAL TAXES.

COMPANY SALES OFFICES AND ENGINEERING REPRESENTATIVES

Alabama
FACT-TRONICS
P.O. Box 1135, Huntsville
(205) 539-7193

RAYTHEON COMPUTER
Holiday Office Center, Suite 8, Huntsville, 35801
(205) 881-2844
TWX 510 579-2113

California
RAYTHEON COMPUTER
2700 South Fairview Street, Santa Ana, 92704
(714) 546-7160
TWX 714 546-0444

WILLIAMS, HEDGE & MARTIN
4341 West Commonwealth, Fullerton, 92633
(714) 521-7410

WILLIAMS, HEDGE & MARTIN
Fayette Townhouse, Suite 308
2675 Fayette Drive, Mt. View
(415) 327-0735

Colorado
AZTEC ENTERPRISES, INC.
3385 S. Bannock St., Suite 103, Englewood, 80110
(303) 761-0101

Florida
FACT-TRONICS
P.O. Box 3202, Orlando, 32802
(305) 423-7069
TWX 305 838-4361

Illinois
PIVAN ENGINEERING
3535 West Peterson Avenue, Chicago, 60645
(312) 539-4838
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Indiana
PIVAN ENGINEERING
10447 North College Avenue, Indianapolis, 46280
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TWX 317 635-5407

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P.O. Box 1274, Cedar Rapids
(319) 365-6635

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880 Bonifant Street, Silver Springs, 20910
(301) 585-3141
TWX 710 825-9635

Massachusetts
RAYTHEON COMPUTER
440 Totten Pond Road, Waltham, 02154
(617) 891-5418
TWX 617 894-8590

Michigan
WKM ASSOCIATES, INC.
1474 East Outer Drive, Detroit, 48234
(313) 892-2500

Minnesota
PIVAN ENGINEERING
3203 North Highway 100, Minneapolis, 55422
(612) 537-4501

Missouri
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7916 Paseo Street, Kansas City, 64131
(816) 444-9494
TWX 816 556-2423

HARRIS-HANSON CO.
2814 South Brentwood Blvd., St. Louis, 63144
(314) 647-4350
TWX 314 962-3933

New Jersey & Met. New York
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2035 Lemoine Avenue, Fort Lee, 07024
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5206-B Constitution NE, Albuquerque, 87110
(505) 268-6421

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3307 Erie Blvd. East, De Witt (Syracuse) 13214
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(716) 835-6186

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Cleveland, 44129
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WKM ASSOCIATES, INC.
6085 Far Hills Avenue, Dayton, 45459
(513) 298-7203
TWX 513 944-0280

Pennsylvania
L. G. WHITE & CO.
100 N. Essex Avenue, Narberth, 19027
(215) 664-6505
TWX 215 667-3949

WKM ASSOCIATES, INC.
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(412) 892-2953
TWX 412 525-2356

Texas
CAREY-WOLF CO.
3327 Winthrop Avenue, Ft. Worth, 76116
(817) 738-1702, -3893
TWX 817 891-8203

CAREY-WOLF CO.
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(713) 643-2114
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Washington
THE THORSON CO.
1767 15th Avenue So., Seattle, 98144
(206) 325-5000
TWX 206 998-0763

Washington, D. C.
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4217 Wheeler Avenue, Alexandria, 22304
(703) 836-7616
TWX 703 931-4247

Wisconsin
PIVAN ENGINEERING
P.O. Box 437, Waukesha, 53187
(414) 547-5131